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# Temperature and Annealing Effects on InAs Nanowire MOSFETs

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**Abstract:**

We report on temperature dependence on the drive current as well as long-term effects of annealing in vertical InAs nanowire Field-Effect Transistors. Negatively charged traps in the $HfO_2$ gate dielectric are suggested as one major factor in explaining the effects observed in the transistor characteristics. An energy barrier may be correlated with an un-gated InAs nanowire region covered with $HfO_2$ and the effects of annealing may be explained by changed charging on defects in the oxide. Initial simulations confirm the general effects on the *I-V* characteristics by including fixed charge.

## 1. Introduction

III-V semiconductors are attractive as channel material due to their high electron velocity and mobility. High performance has been show by $In_xGa_{1-x}As$ High Electron Mobility Transistors (HEMTs) with maximum oscillation frequencies, $f_{max} > 1$ THz and transconductance, $g_m > 2$ mS/mm [1]. The disadvantage with HEMTs is the comparably large gate leakage currents. Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with high-*k* gate dielectric does not suffer from this and still show good performance. One example is the $In_{0.7}Ga_{0.3}As$ FET with $TaSiO_x$ gate dielectric showing $g_m = 1.75$ mS/mm [2]. As the scaling of transistor dimensions continue, nanowires has turned out to be a promising structure as it allows for improved electrostatic control of the channel. Compared to planar devices, nanowire structures also allows for thicker body and gate oxides [3].

We use arrays of vertical InAs nanowire as the channel material in MOSFETs with high-$k$ gate dielectric and wrap contacts [4]. $g_m$ = 0.6 mS/mm and subthreshold slope of 80 mV/decade has been reported [5]. Recently, the technology has been transferred to Si substrates by a InAs buffer layer technology [6]. The resiliency against defects in the vertical nanowire geometry enables good crystal quality, but improved integration of high-$k$ both in terms of oxide quality and the semiconductor-oxide interface quality is required to improve the device characteristics.

In this paper, electrical characterization of vertical InAs nanowire MOSFETs at different temperatures are presented together with a study of the long term effects of annealing. It is suggested that negative charge traps in the $HfO_2$ have a major influence on the transistor characteristics. This is also modeled in initial simulations by adding fixed charges in the $HfO_2$.

## 2. Device Fabrication

Vertical InAs nanowire arrays are integrated on a highly resistive Si<111> substrate by a InAs buffer layer. The nanowires act as the channel material of the transistors and we use the epitaxial InAs layer as source contact. Moreover, $HfO_2$ is used as gate dielectric, a W wrap contact is used as gate, and a Ti/W/Au contact is used as drain. The technology is described in detail elsewhere [6], [7]. The vertical device is illustrated by a schematic image and a cross-sectional scanning electron microscopy (SEM) image in Figure 1 a and b.

The structure was realized by first growing a 290 nm thick epitaxial InAs layer by Metal Organic Vapor Phase Epitaxy (MOVPE) on the highly resistive Si <111> substrate [8]. A mobility of 2560 $cm^2$/Vs and a charge carrier concentration of $2.4 \cdot 10^{18}$ $cm^3$ was measured for the InAs layer by Hall measurements. Arrays of Au particles were defined on the InAs layer by Electron Beam Lithography (EBL) and used to facilitate Vapor Liquid Solid (VLS)-

assisted growth of about 1 μm long InAs nanowires with diameters of 35 nm [9]. The nanowires were n-type doped by incorporation of Sn. The Sn molar fraction of $1.1\cdot10^{7}$ corresponds to a doping of $2\cdot10^{18}$ $cm^{-3}$ [10]. After nanowire growth, the sample was transferred to a Atomic Layer Deposition (ALD) chamber without any chemical pre-treatment. 80 cycles (about 5-7 nm) $HfO_2$ was deposited at 250°C with tetrakis(dimethylamino)hafnium (TDMA-Hf) and water precursors in a Savannah-100, starting with a TDMA-Hf pulse.

An organic spacer for source-gate isolation was deposited and thinned down to about 200 nm. On top of the organic spacer, a W gate metal was deposited by sputtering. The wrap-gate length set by dry etching in a $SF_6$/Ar ambient to about 300 nm. A second organic spacer for gate-drain isolation was deposited and thinned down. The spacer was also used as an etch mask when removing the gate dielectric from the upper part of the nanowires in buffered oxide etch (BOE). Finally, a Ti/W/Au top metal layer was deposited by sputtering and patterned with UV-lithography. All layers were also patterned with UV-lithography to enable electrical measurements. For the source and gate, connections to the top metal layer were made through vias in the organic spacers.

## 3. Measurements and Results

### 3.1 Temperature dependence

Transistors with nominally 52 nanowires in parallel were electrically characterized by on-chip probing in a Cascade 1100B probe station at different temperatures (125°C, 55°C, 25°C, 0°C and -55°C). Figure 2 show a comparison of the output characteristics (*I-V*) for the highest (125°C) and lowest (-55°C) temperature with the source contact connected to ground in Figure 2a (common source configuration) and drain contact connected to ground in Figure 2b (common drain configuration). The *I-V* show increasing currents with increasing temperature in both bias directions. This temperature dependence indicates the presence of at least one

energy barrier between source and drain. Moreover, the *I-V* is more symmetric at higher temperatures; at 125°C the current is about two times higher with drain connected to ground, but almost ten times higher at -55°C. Good fit in Arrhenius plots of the measured current indicate that the barrier can be modeled using a standard expression for thermionic emission:

$$I \propto T^2 \cdot \exp\left(-\phi_B / kT\right) \quad (1)$$

Here, $I$ is the current, $\phi_B$ is the barrier height, $T$ is the temperature and $k$ is Boltzmann's constant. The activation energy related to the barrier height can then be deduced from the slope in an Arrhenius plot. The resulting barrier height is plotted as a function of drain/source voltage, $V_{d/s}$, and for different gate voltages, $V_g$ in Figure 3. For sufficiently high $V_{d/s}$ and positive $V_g$, an energy barrier of about 80 meV is deduced when the transistor is biased with source connected to ground, but not when drain is connected to ground. This implies that the energy barrier is situated between the gate and source. We cannot exclude the possibility that there might also be a smaller energy barrier between gate and drain, but the effect of such a barrier would be smaller. The barrier height was deduced for two more nominally identical devices, showing the same source-drain dependence with barrier heights of about 80 meV and 110 meV, respectively.

Asymmetry is observed in the coverage of $HfO_2$ along the nanowires from cross-sectional scanning electron microscopy (SEM) images (such as Figure 1b); the $HfO_2$ gate dielectric is present only underneath the gate and below the gate contact, whereas the un-gated part of a nanowire above the gate is not covered with $HfO_2$. This suggests negative charge traps in the $HfO_2$ as an origin of the measured energy barrier. Furthermore, a comparison of the currents for the two bias configurations show a leakage through the substrate of a few μA. This current can, however, be considered negligible in relation to the observed asymmetry in the *I-V*.

### 3.2 Long Term Annealing Effects

The long term annealing effects on the transistor characteristics was studied by repeated

measurements of the on-current, $I_{on}$, at room temperature (RT). Measurements were performed before and after annealing and, then, repeatedly with a few days interval until the effects of the annealing could no longer be seen. In Figure 4, the on-current at RT, and at $V_{gs}$ = 1 V and $V_{ds}$ = 1 V is plotted versus time. The chip was annealed in total four times; two times in a heated probe station at 125°C and, after that, two times on a hotplate at 200°C. Between the measurements, the chip was mainly stored in vacuum. As seen in Figure 4, the current increases considerably when the chip is annealed; the increase is about 10 times when annealed at 200°C. Hereafter, the on-current slowly decreases and reaches a steady-state lower level after some weeks. We suggest that also this behavior might be attributed to negative charge traps in the $HfO_2$. The behavior may be seen as charge traps being emptied when the chip is annealed and then slowly filled up with a very low capture rate. The very long time constant, in the order of several days, indicates that the traps are situated deeply inside the insulting layer and not in the semiconductor itself. The origin of the behavior may be structural changes in the high-*k* film during the annealing process that are not stable over time, and influence the charge trap states. Similar effects attributed to negatively charged traps have also been suggested to give a high source resistance in lateral FETs [11].

**5. Modeling**

A simple drift-diffusion model of the transistor was used to simulate the effect of charge traps on the *I*-*V* characteristics, using ATLAS by Silvaco. The model consists of a wrap-gated n-type InAs nanowire ($\mu_n$ = 4000 $cm^2$/Vs, $v_{sat}$ = $3\cdot10^7$ cm/s) with 8-nm-thick $HfO_2$ gate dielectric. Besides from the 250 nm long gated region, the nanowire also has two 250 nm long un-gated regions; one covered with high-*k* (defining this side as source) and one without high-*k* (defining this side as drain). The nanowire is embedded in a low *k* material, and has a metallic contact to the nanowire at the drain. At the source, the nanowire is contacted through an InAs film. Both the nanowire and the InAs film have a doping of $2\cdot10^{18}$ $cm^{-3}$. The charge

traps are simulated by placing fixed negative charge with a concentration of $2 \cdot 10^{12}$ $cm^{-2}$ at the external high-*k* interface in the un-gated region. The resulting *I-V* characteristics for the two bias directions and 52 nanowires in parallel are shown in Figure 5 and compared to the measured data. Previous experiments have shown that the current scales roughly linearly with the number of nanowires.

The asymmetry of the two bias directions is recognized from the experimental *I-V* characteristics; the currents are lower in common source configuration and the output conductance higher in common drain configuration. A simulation without any charge traps give symmetric transistor behavior with an on-current of about 50 μA per nanowire, as compared with about 5 μA for grounded source and 0.6 μA for grounded drain for a device with defects.

**6. Conclusion**

We have studied the temperature dependence of InAs nanowire MOSFETs and found that a barrier between source and gate is dominating the temperature dependence. This can be correlated to an un-gated part of the nanowire that is covered with $HfO_2$. Trapped negative charges in the $HfO_2$ are suggested as an explanation of this temperature dependence. Long term studies following annealing show increased on-currents after the annealing and a very slow decrease to the original current level. This may also be attributed to discharging of the trapped negative charges and to the long term stability of the defects. Simulations of the output characteristics including negative charges in the $HfO_2$ confirm the major effects seen experimentally.

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**Captions :**

*Fig. 1: The vertical structure of the InAs nanowire MOSFET illustrated by a schematic (a) and by a cross-sectional SEM image (b). The SEM image is realised by cleaving a reference sample processed in parallel with transistor samples.*

*Fig. 2: Output characteristics of a nanowire MOSFET at two different temperatures (125°C and -55°C) with source connected to ground in (a) and with drain connected to ground in (b). The insets show I-V characteristics for -55°Cat a different scale.*

*Fig 3: Barrier height as a function of drain/source voltage. The drain voltage is defined as a positive voltage in commons source configuration and the source voltage is defined as negative voltage in the common drain configuration. The gate voltage is stepped between -1.5 V and 1.5 V.*

*Fig 4: The on-current of a transistor measured at RT plotted versus time, showing the long term effects of annealing. The transistor is biased at* $V_{gs} = 1$ *V and* $V_{ds} = 1$ *V with source connected to ground. The sample was annealed four times during this time period as indicated by red arrows.*

*Fig 5: Simulated I-V characteristics for a 52-nanowires-transistor at room temperature with fixed negative charges at the external high-k interface (solid lines) is compared to measured data for a nominally-52-nanowires-transistor at room temperature, and,* $V_g = 0$ *(dashed lines).*