InGaAs Nanowire and Quantum Well Devices

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InGaAs Nanowire and Quantum Well Devices

Doctoral Thesis

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LUND
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Department of Electrical and
Information Technology
Lund, June 2022

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Abstract

To fulfill the increasing demand for high-speed electronics used for computation or communication is one everlasting challenge for the semiconductor industry. Emerging fields such as quantum computation also has a need for circuits operating at cryogenic temperatures. The metal-oxide-semiconductor field-effect transistor (MOSFET) is the main component in modern electronics, traditionally fabricated in Si. However, III-V materials generally exhibits higher electron mobility compared to Si. This enables the realization of MOSFETs with higher operational speed or lower power consumption. While a nanowire geometry, where the channel is gated from multiple sides brings an increase in the electrostatic gate control, allowing for further gate length scaling. In this thesis, lateral InGaAs nanowire and quantum well devices have been fabricated and characterized with the purpose of understanding the electron transport and its limitations over a wide temperature range. MOSFETs at cryogenic temperatures, where the phonon occupation is low, are highly sensitive to disorder and defects in the semiconductor/oxide interface. InGaAs RF MOSFETs with different spacer technologies for reducing capacitances have also been fabricated and characterized. Optimizing the spacers for low capacitance and low access resistance is a key design consideration when fabricating devices for high-frequency operation.

Populärvetenskaplig Sammanfattning

De första elektriska datorerna byggdes av elektronrör och kunde fylla ett helt rum, men idag har vi en dator många gånger mer kraftfull som får plats i fickan, mobiltelefonen. Denna enorma utveckling de senaste 80 åren har framför allt drivits av den ständiga utvecklingen av kiseltransistorer och den integrerade kretsen.

En transistor är en halvledarkomponent med tre anslutningar eller elektroder, där en av elektroderna kontrollerar hur mycket ström som går mellan de andra två elektroderna. Det fungerar ungefär som en ventil i en vattenkran, där positionen på handtaget kan styra mängden vatten som kommer igenom. Inom elektroniken kan transistorer användas till väldigt många olika saker, det är den viktigaste (och vanligaste) komponenten i alla dagens kretsar. De kan användas i digitala kretsar för att representera ettor och nollor. Detta är grunden för beräkningsprocessorer till exempel i en dator eller mobiltelefon. De används som minnen i datorer för att kunna spara all data. De kan också användas för att filtrera och förstärka signaler, detta är väldigt centralt i till exempel trådlös kommunikation.

De första kiseltransistorerna var relativt stora, men i moderna transistorer är vissa kritiska dimensioner bara några få nanometer. Det finns många anledningar till att skala ner transistorernas storlek, den mest uppenbara är att man kan få plats med fler på samma chip. Men det finns även andra fördelar, de blir också snabbare vilket innebär att man kan göra fler beräkningar varje sekund eller behandla signaler med högre frekvens. En mindre transistor kan också drivas med mindre spänningen, vilket sparar energi. Idag kan man tillverka kretsar med flera miljarder transistorer tillsammans med andra

passiva komponenter på bara ett fåtal kvadratmillimeter. Dagens transistorer går nästan inte att göra mindre, detta har lett till att man utforskar om man kan använda sig av andra material än kisel. Ett av dessa material är III-V halvledare, vilket är sammansatt av grundämnen från grupp tre och grupp fem i det periodiska systemet, till exempel indium-gallium-arsenid som ofta skrivs som InGaAs. I dessa typer av halvledare kan strömmen generellt flyta lättare, vilket innebär att man kan bygga transistorer som är både snabbare och använder mindre energi.

På senare år har intresset ökat för nya applikationer där transistorer används, till exempel i kvantdatorer. I den kallaste delen av en kvantdator är det nästan lika kallt som vid absoluta nollpunkten, alltså -273 °C, detta ställer helt andra och olika krav på transistorerna. Denna avhandling omfattar design och tillverkning av InGaAs nanotrådstransistorer och kvantbrunn komponenter. Komponenterna har kylts ner till kryogeniska temperaturer för att undersöka elektrontransportens egenskaper jämfört med rumstemperatur.

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During my time in Lund, I have had the opportunity to interact and collaborate with many inspiring people. First, I would like to extend my gratitude to my main supervisor, *Erik Lind*. Thank you for guiding me during my studies and thank you for all the fruitful and encouraging discussions. Your door has always been open, and you have been answering my barrage of questions with great knowledge and enthusiasm. I would also like to thank my second supervisor *Mattias Borg*, for your scientific insight and advice throughout the years. I would also like to thank *Lars-Erik Wernersson* for providing a great research environment. To *Johannes Svensson*, thank you for all the support inside the clean room.

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Finally, I would also like to thank my family, who have always encouraged and supported me during my studies.

Lasse Södergren
Lund, June 2022

Contents

Preface

This thesis is the culmination of five years of work in the *Electromagnetics & Nanoelectronics* division at the department of Electrical and Information technology at Lund University. The work was supervised by Associate Professor *Mattias Borg* and Professor *Erik Lind*.

STRUCTURE OF THE THESIS

- **INTRODUCTION**
  The main body of the thesis consists of the publications appended in the back. The introduction provides a broader and more comprehensive view than the very focused publications and ties their work together. The introduction is intended to be comprehensible for aspiring researchers with a Master's degree in physics or a related subject.

- **APPENDICES**

  A InGaAs MOSFET Fabrication Process
  Appendix A provides a detailed description of the InGaAs MOSFET fabrication process.

- **PAPERS**
  The papers forming the main body of the thesis are reproduced in the back and listed in the following.

INCLUDED PAPERS

The following papers form the main body of this thesis and the respective published or draft versions are appended in the back.

Paper I: L. Södergren, N. S. Garigapati, M. Borg and E. Lind, "Mobility of near surface MOVPE grown InGaAs/InP quantum wells", *Applied Physics Letters*, vol. 117, no. 1, pp. 013102, 2020, doi: 10.1063/5.0006530.

► *I designed, performed the semiconductor growth, fabricated and measured the devices. I did the data analysis and wrote the paper.*

Paper II: N. S. Garigapati, L. Södergren, P. Olausson and E. Lind, "Strained $In_xGa_{1-x}As$/InP near surface quantum wells and MOSFETs", *Applied Physics Letters*, vol. 120, no. 9, pp. 092105, 2022, doi: 10.1063/5.0073918.

► *I performed the semiconductor growth. I co-fabricated the devices and performed the measurements.*

Paper III: P. Olausson, L. Södergren, M. Borg and E. Lind, "Optimization of Near-Surface Quantum Well Processing", *Physica Status Solidi A*, vol. 218, no. 7, pp. 1862-6300, 2021, doi: 10.1002/pssa.202000720.

► *I performed the semiconductor growth, co-fabricated the devices, collaborated in developing the process steps and performed part of the measurements.*

Paper IV: N. S. Garigapati, F. Lindelöw, L. Södergren and E. Lind, "Capacitance Scaling in $In_{0.71}Ga_{0.29}As$/InP MOSFETs With Self-Aligned a:Si Spacers", *IEEE Transactions on Electron Devices*, vol. 68, no. 8, pp. 3762-3767, 2021, doi: 10.1109/TED.2021.3092299.

► *I performed the semiconductor growth and co-fabricated the devices.*

Paper V: F. Lindelöw, N. S. Garigapati, L. Södergren, M. Borg and E. Lind, "III-V nanowire MOSFETs with novel self-limiting Λ-ridge spacers for RF applications", *Semiconductor Science and Technology*, vol. 35, no. 6, pp. 065015, 2020, doi: 10.1088/1361-6641/ab8398.

► *I performed the semiconductor growth and co-fabricated the devices. I was also a part of developing the process steps.*

Paper VI: L. Södergren, P. Olausson and E. Lind, "Low-Temperature Characteristics of Nanowire Network Demultiplexer for Qubit Biasing", *Nano Letters*, 2022, doi: 10.1021/acs.nanolett.1c04971.

► *I designed, performed the semiconductor growth, fabricated and measured the devices. I did the data analysis and wrote the paper.*

Paper VII: L. Södergren, P. Olausson and E. Lind,

"Cryogenic Characteristics of InGaAs MOSFET", manuscript in progress.

► *I performed the semiconductor growth, fabricated and measured the devices. I performed the data analysis and wrote the paper.*

Paper VIII: Y. -P. Liu, L. Södergren, S. F. Mousavi, Y. Liu, F. Lindelöw, E. Lind, R. Timm and A. Mikkelsen, "Low temperature scanning tunneling microscopy and spectroscopy on laterally grown $In_xGa_{1-x}As$ nanowire devices", *Applied Physics Letters*, vol. 117, no. 16, pp. 163101, 2020, doi: 10.1063/5.0021520.

► *I performed the semiconductor growth and fabricated the devices. I was involved in the data analysis and wrote part of the paper.*

INTRODUCTION

1

Background

1.1 BRIEF HISTORY OF THE TRANSISTOR

In the modern era where human society is interconnected with a lot of different electrical applications, the transistor is one of the most important components in circuits. Billions of transistors are present in the central-processing-unit (CPU) in everyday computers and smartphones, or in the servers creating the internet connecting the world. They are also used in wireless communication, power supplies and as sensors. It all started at Bell laboratories in 1947 where the first transistor was invented by John Bardeen, Walter Brattain and William Shockley [1]. This point-contact transistor was basically two gold contacts closely spaced on a layer of germanium situated on a base copper contact. Current through one gold contact and the base controlled a much larger current through the other gold contact, they had created a current amplifier. This design was later replaced by more reliable bipolar junction transistors (BJT) and field-effect transistors (FET). The first working metal-oxide-semiconductor field-effect transistor (MOSFET) was demonstrated in 1959. Silicon semiconductor technology advancement and the invention of the integrated circuit (IC) and the complementary MOS logic (CMOS), has transformed the first bulky MOSFETs to modern implementation of billions of MOSFETs on the same chip [2].

1.2 BASIC MOSFET OPERATION

The MOSFET is a device with three terminals, the source, drain and gate. Figure 1.1(a) shows a schematic of an n-channel bulk MOSFET. The gate is isolated from the semiconductor by a thin gate oxide, so in the ideal case no current can flow through the gate. The source/drain contacts are placed on highly n-doped semiconductor in order to create a good ohmic contact. In the highly n-doped regions the Fermi level is close to the conduction band edge and there is a large electron concentration in the source. The path between the source and drain is called the channel, the gate potential controls the conductivity of the channel by raising or lowering the potential energy barrier. Figure 1.1(b) shows a schematic band diagram of the MOSFET. In the off-state there is a high potential barrier which the majority of the electrons do not have the thermal energy to overcome. By applying a positive bias on the gate electrode, the potential energy will be reduced, via an electric field through the gate oxide. This allows more electrons to flow between the source/drain contact. If a positive bias of $V_{DS} > 0$ V is applied there will be a net flow of electrons entering the drain, the transistor is then in the on-state. The voltage at which the device switches between the off-state and on-state is called the threshold voltage V_T. In a real MOSFET, the gate current is not strictly zero since there is some leakage current through the gate oxide.

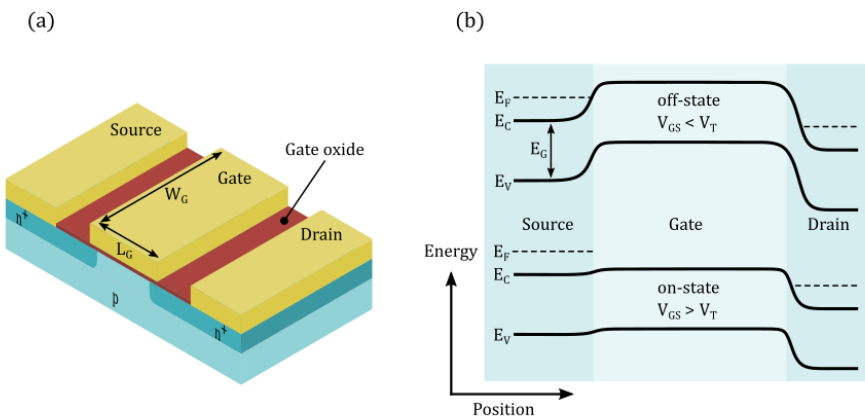

Figure 1.1: a) Schematic of a n-channel planar MOSFET structure. b) Energy band diagram of the MOSFET along the gate length in both the off-state and the on-state.

The DC performance of a MOSFET is determined by measuring the relation between applied voltages and currents. Figure 1.2 shows two examples of

common I-V curves used to characterize a MOSFET. The transfer characteristics which show the dependence of the drain current I_{DS} on the gate-to-source voltage V_{GS}, under a fixed source-drain bias voltage V_{DS}. The output characteristics show the I_{DS} dependence on V_{DS}. To be able to compare different sizes of transistors, the current is often normalized to the gate width, or to the gated perimeter for tri-gate or gate-all-around (GAA) structures. The transconductance g_m is the derivative of the transfer characteristic, defined as $g_m = \partial I_D / \partial V_{GS}$. This is an important metric for the on-state performance of the MOSFET since it determines the gain the device can provide. High g_m is crucial for the performance in high-frequency applications. The threshold voltage is often determined by an intersect of the linear extrapolation of I_D from the point of maximum g_m and the gate voltage axis. An alternative way to find V_T is to look at the peak of the second derivative of I_D with respect to V_{GS}. The off-state performance is characterized by the inverse subthreshold slope, $S = (\partial log(I_D)/\partial V_{GS})^{-1}$. This describes how well the gate can turn of the transistor, for a MOSFET which relies on thermionic emission over an energy barrier this has a theoretical minimum of $S = 60$ mV/decade at room temperature. The off-state current is defined to some value, for example 1 nA/μm, which is dependent on the application. A low obtainable off-current and a low inverse subthreshold slope are important for low power applications, since it facilitates the use of a lower supply voltage V_{DD}. The

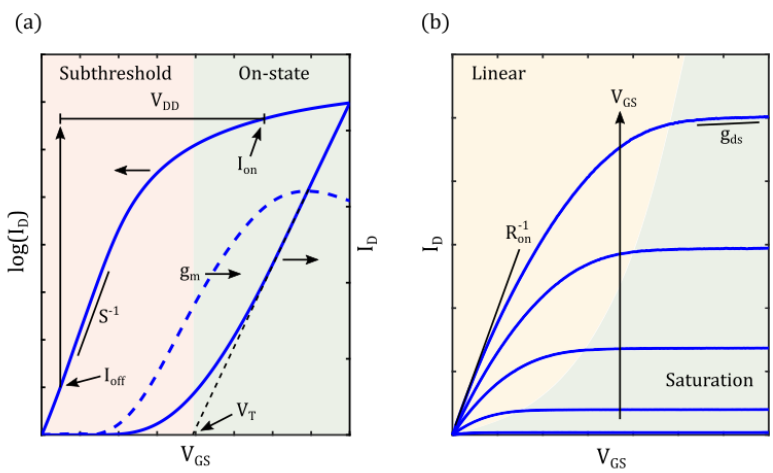

Figure 1.2: I-V curves to characterize MOSFETs, important metrics are indicated with the procedure to extract them. (a) Transfer characteristics, drain current dependence on V_{GS}. (b) Output characteristics, drain current dependence on V_{DS} for different V_{GS}.

on-current can then be found by starting from the off-current and moving along the transfer curve a distance equal to the intended drive voltage. The output conductance g_{ds} is found by the slope in the output characteristics while the transistor is in saturation ($V_{DS} > V_{GS} - V_T$). Finally, the on-resistance R_{on} is the invers of the slope at low V_{DS} (linear region) using the output characteristics. The on-resistance is the sum of the channel resistance and the access resistance R_S and R_D attributed to the source and drain side respectively.

For radio frequency (RF) applications, a high g_m is important for good high-frequency performance. However, it is also important to minimize the extrinsic capacitances which are detrimental to the performance. The transition frequency which is defined as the frequency where the current gain is unity, can be approximated as [3]

$$f_T \approx \frac{1}{2\pi}\left(\frac{C_{gs}+C_{gd}}{g_m} + C_{gd}(R_S+R_D)\right)^{-1}. \tag{1.1}$$

The capacitances C_{gs} and C_{gd} are the respective gate-source and gate-drain capacitances (including both intrinsic and extrinsic capacitances). R_S and R_D are extrinsic resistances attributed to the source- and drain-side respectively. Minimizing these access resistances often leads to an increase of the extrinsic capacitances due to the geometry of the MOSFET. Designing spacer structures which minimizes both access resistances and extrinsic capacitances is crucial for high-frequency performance. Another metric describing the RF capabilities is the maximum oscillating frequency, given as [4]

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi R_G\left(C_{gd}+\frac{C_{gg}g_{ds}}{g_m}\right)}}, \tag{1.2}$$

which is the frequency where the power gain is unity. From these simplified expressions the importance of high g_m, low capacitances and low access resistance are highlighted. For f_{max} it is also important to minimize the gate resistance R_G and the output conductance g_{ds}.

1.3 MATERIALS AND SCALING

A constant increase of Si transistor performance over the years has traditionally been achieved by scaling the MOSFET dimensions. By scaling the gate length L_G, the width W_G, the gate oxide thickness t_{ox} aswell as the supply voltage V_D with a factor $1/\kappa$, the switching delay is reduced by $1/\kappa$ while keeping a constant power density. This is known as Dennard scaling [2, 5].

This scaling led to the famous Moore's Law, which predicted that the number of transistors in an integrated circuit will double roughly every second year [6]. The advancement of the Si transistor technology has enabled higher clock frequencies and transistor density which is the reason for the high computing power in modern integrated circuits [7, 8]. At very short gate lengths the gate might lose electrostatic control of the channel and the drain voltage will also impact the current. This may lead to short channel effects such as drain induced barrier lowering (DIBL) and higher off-currents. To combat this, the gate oxide thickness t_{ox} is also scaled, but at some point, the oxide will be thin enough so quantum tunneling through the gate oxide will become an issue.

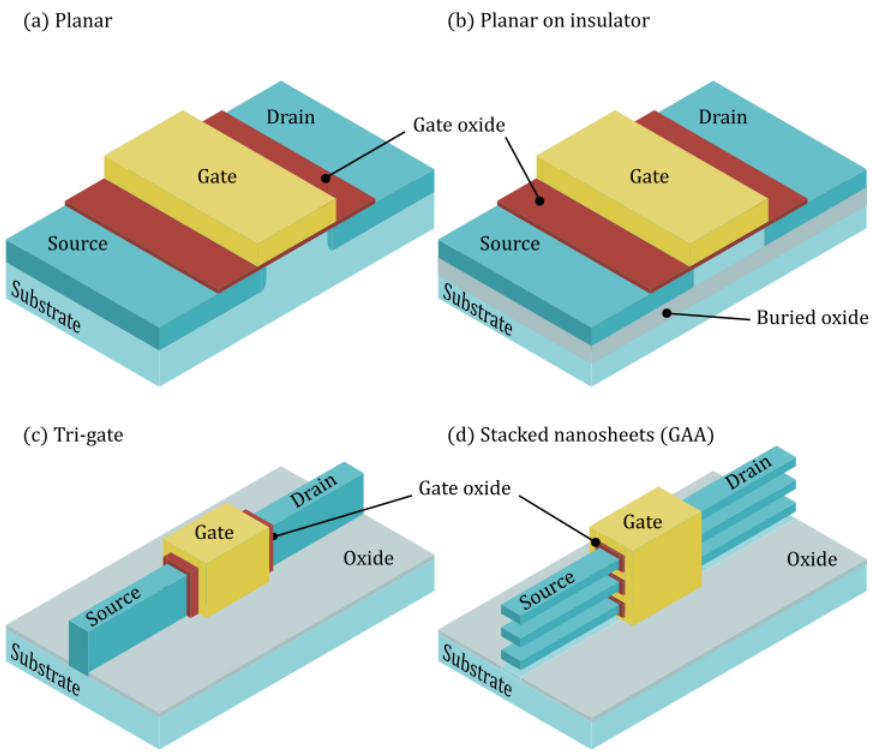

Figure 1.3: Schematic of different MOSFET geometries. (a) Traditional planar design. (b) Planar on insulator design where a buried oxide is inserted to limit substrate leakage currents. (c) Tri-gate design with improved electrostatic control due to gating of the channel from three sides. (d) Stacked nanosheet architecture which enables the gate to surround the channel in a gate-all-around design for even better electrostatic control.

This leads to gate leakage currents which increases the power consumption. This was a fundamental challenge, which limited the geometric scaling of device dimensions. It was solved by changing the gate oxide to an oxide with a higher relative permittivity ϵ_r, which allows for higher capacitance with a thicker oxide, $C = \epsilon_0\epsilon_r/t_{ox}$ [9, 10]. This allows for the use of a thicker gate oxide which limits the gate leakage. In a very short gate length device, the channel also has to be thin to maintain sufficient electrostatic control. This introduces other challenges such as quantization effects and reduced electron mobility due to surface roughness scattering [11].

The electrostatic control can also be improved by changing the transistor geometry [12–15]. Figure 1.3 shows schematics of the transistor geometry development. The buried oxide in the silicon-on-insulator structure suppresses leakage current far from the gate electrode where the electric field is weaker. By gating the channel from multiple sides as in the tri-gate or gate-all-around device, the electrostatic control can be improved, allowing for a design with thicker gate oxide and thicker/shorter channel. The high aspect ratio channels also have the benefit of increased drive current per chip area.

The electron mobility is a parameter which describes how easy the electrons move in an electric field. Higher mobility channel material is advantageous for building a MOSFET with high g_m and I_{on}. III-V semiconductors generally exhibit higher electron mobilities and lower effective mass compared to Si, which makes them a good candidate for high-speed transistors [16]. The actual effective mobility in MOSFETs is often reduced due to scattering from defects in the semiconductor/oxide interface or inside the oxide. It has proven to be more challenging to obtain semiconductor/oxide interfaces with low defect density in III-V compared to Si [17, 18]. There are also other emerging materials such as carbon nanotubes and 2D materials such as graphene or transition metal dichalcogenides.

1.4 MOTIVATION

The thesis aims to provide understanding of the transport in selective area grown InGaAs nanowire and quantum well devices over a wide temperature range. The near surface quantum well structure is present in MOSFETs either in the channel region or as ungated access regions. The balance between access resistance and capacitances is important in design of high-frequency MOSFETs. Investigation of the transport properties and limitations at cryogenic temperatures is important for understanding the operation of devices relevant for applications such as quantum computing [19–21]. Chapter 2 introduces theory used to explain electron transport. Namely a model describing a 1D ballistic transport relevant for highly scaled MOSFETs, and

electron scattering in a 2D quantum well. Chapter 3 describes the fabrication modules used for InGaAs nanowire/quantum well MOSFETs. This includes the InGaAs growth process and the different process modules used to fabricate contacts, gate and dielectric layers. Chapter 4 summarizes the included papers by discussing some of the findings.

2

MOSFET Theory

In this chapter, the most important concepts describing the electron transport through a MOSFET will be summarized.

2.1 DRIFT AND DIFFUSION

Classical transport of carriers through a semiconductor can be described by drift and diffusion transport [22,23]. The current density is given as

$$J = qn\mu\frac{\partial E_F}{\partial x}. \tag{2.1}$$

Using the Boltzmann approximation this becomes the familiar drift and diffusion equation,

$$J = qn\mu E_x + qD\frac{\delta n}{\delta x}, \tag{2.2}$$

with the Einstein relation $D = \mu k_B T_L/q$. The first term is drift current which is driven by the electric field (difference in potential), the second term is a diffusive current driven by the difference in carrier concentration. The mobility μ is a material parameter describing how easy the electrons move in an electric field E_x. This is inversely proportional to the electron effective mass. Considering transport of drift transport as in a large MOSFET, the current can be written as

$$I_{D,lin} = \frac{W_G}{L_G}C_{gs}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right), \tag{2.3}$$

in the linear region ($V_{DS} < V_{GS} - V_T$). This is ignoring the diffusive current above threshold, which is a valid assumption since it is much smaller than

the drift current. The dimensions W_G and L_G are the width and length of the channel as in figure 1.1 and C_{gs} is the gate-source capacitance, which can in the simplest case be approximated as the oxide capacitance C_{ox}. When devices are scaled to very small gate lengths the applied electric field become very large and the electron velocity ($v = \mu E_x$) tends to saturate at some finite value v_{sat} [24]. This is due to an increased scattering rate of the very high energetic carriers. Including velocity saturation and assuming a short channel device, the drain current in the saturation regime ($V_{DS} > V_{GS} - V_T$) is

$$I_{D,sat} \approx W_G C_{gs} v_{sat} (V_{GS} - V_T). \tag{2.4}$$

2.2 MOSFET ELECTROSTATICS AND 1D BALLISTIC TRANSPORT

With a high electron mobility channel, the average time between scattering events can be long enough so the electron can move through the device without any scattering event. In other words, if the mean free path is longer than the gate length the transport can be approximated as ballistic transport. In a scaled nanowire device, the electrons are confined in two directions and only free to move in the third direction. The source and drain are seen as electron reservoirs where strong scattering occurs. Both reservoirs inject electrons into the channel, some which reflect on the potential barrier and some which reaches the opposite reservoir without experiencing any scattering. This leads to a special condition at the top of the barrier where all positive k-states are in equilibrium with the source and all negative k-states are in equilibrium with the drain [25]. This is a simplification since in a real MOSFET, which can be seen as quasi-ballistic some scattering always occurs which will mix the two thermal equilibriums. The electron density in each subband can be calculated from the density of states (DOS) and the probability of each state's occupation as

$$n_0 = \int D(E) f_0(E, E_F) dE, \tag{2.5}$$

where f_0 is the Fermi-Dirac distribution. In a 1D system in an effective mass approximation with parabolic bands the density of states is given by

$$D_{1D}(E) = \frac{\sqrt{2m^*}}{\pi\hbar\sqrt{E - E_C}}. \tag{2.6}$$

At the top of the barrier, since all the electrons are in equilibrium with the reservoir they originated from, the charge can easily be divided into two parts. The part originating from the source can be written as

$$n_0^+ = \frac{N_{1D}}{2} \mathcal{F}_{-1/2}(\eta_F), \tag{2.7}$$

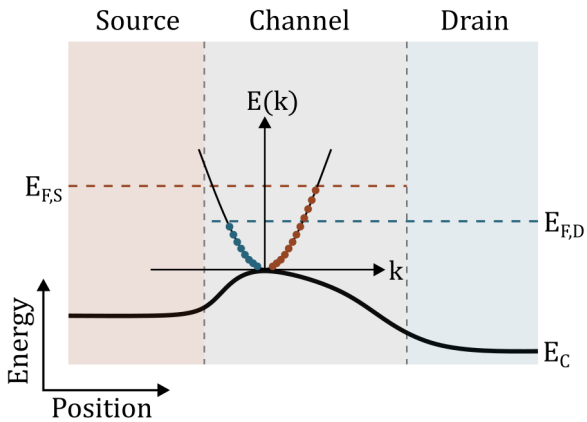

Figure 2.1: Schematic diagram of the situation at the top of the barrier in a fully ballistic MOSFET. Since no scattering occurs, all the positive k-states are in equilibrium with the source and all the negative k-states are in equilibrium with the drain.

with $\eta_F = (E_{F,S} - E_0)/k_B T_L$ where $E_{F,S}$ is the source Fermi level and E_0 is the potential at the top of the barrier. $N_{1D} = \sqrt{2m^* k_B T_L/\pi\hbar^2}$ is the effective density of states and $\mathcal{F}_{-1/2}$ is the Fermi-Dirac integral of order -1/2. The electron density associated with the drain contact are written in a similar way as

$$n_0^- = \frac{N_{1D}}{2}\mathcal{F}_{-1/2}(\eta_F - U_D), \tag{2.8}$$

with $U_D = qV_D/k_B T_L$. Since at an applied bias the drain Fermi level is shifted by $-qV_D$ with respect to the source Fermi level. The total charge at the top of the barrier is then simply the sum of the two components,

$$n_0 = n_0^+ + n_0^-. \tag{2.9}$$

To find the potential E_0 at the top of the barrier, the electrostatics of the system have to be considered. The potential can intuitively be modeled with three capacitors as in figure 2.2. The system can be solved by using superposition. If we first assume that there are no mobile charges ($n_0 = 0$), in the channel, using circuit analysis the potential should then be

$$E_0^a = -q\left(\frac{C_G V_G}{C_\Sigma} + \frac{C_S V_S}{C_\Sigma} + \frac{C_D V_D}{C_\Sigma}\right), \tag{2.10}$$

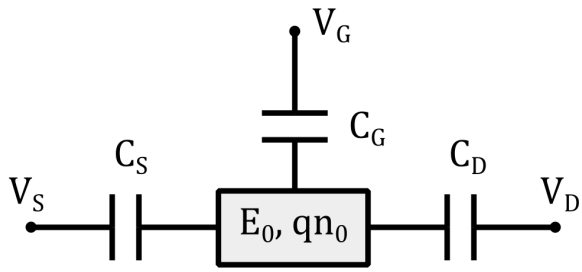

Figure 2.2: Capacitor model for the 2D electrostatic situation in a MOSFET. Three capacitors associated with source, drain and gate control the potential E_0 and the charge qn_0 at the top of the barrier.

where C_Σ is the total capacitance. If instead the voltages are set to zero, then the potential will be set by the mobile charges as

$$E_0^b = \frac{q^2 n_0}{C_\Sigma}. \tag{2.11}$$

In a well behaved MOSFET the gate channel capacitance C_G is much larger than both C_S and C_D and the potential can be approximated as

$$E_0 = E_0^a + E_0^b = -qV_G + \frac{q^2 n_0}{C_G}. \tag{2.12}$$

Since n_0 depends on the potential, equations 2.5 and 2.12 have to be solved iteratively until convergence. Equation 2.10 can explain short channel effects. At short gate lengths C_D can become a substantial part of the total capacitance, this will lower the potential barrier which will result in threshold voltage roll-off. An increased C_D also means that the drain voltage will impact the top of the barrier potential, increasing the drain voltage would decrease the potential at the top of the barrier, which is called drain induced barrier lowering (DIBL).

The gate capacitance is a series combination of the geometric capacitance C_{ox}, the quantum capacitance C_q and the charge centroid capacitance C_c,

$$C_G = \left(\frac{1}{C_{ox}} + \frac{1}{C_q} + \frac{1}{C_c} \right)^{-1}. \tag{2.13}$$

The geometric capacitance is dependent on the permittivity ϵ_{ox}, the thickness of the oxide and the geometry. It can be expressed as $C_{ox} = \epsilon_{ox}\epsilon_0/t_{ox}$ in the simplest form. The charge centroid capacitance takes into account

quantization of charges in the channel [3,26]. The quantum capacitance relates how the mobile charges in the channel changes with the surface potential, under degenerate conditions with high drain bias it becomes,

$$C_q = -q^2 \frac{dn_0}{dE_0} = q^2 \frac{\sqrt{2m^*}}{\pi\hbar\sqrt{E_{F,S} - E_0}} = -q^2 D_{1D}. \tag{2.14}$$

The quantum capacitance is proportional to the density of states which is dependent on the effective mass. With a thick oxide or a large effective mass as in silicon, $C_{ox} << C_q$ and the quantum capacitance could be neglected in equation 2.13. The device would operate in the MOS limit where the gate voltage would have a reduced effect on the barrier potential. In a scaled III-V MOSFET with low effective mass and thin gate oxide, $C_{ox} >> C_q$ and C_{ox} can be neglected. Such a device operates at the quantum capacitance limit (QCL), where the gate directly controls the potential at the top of the barrier and further scaling the oxide thickness would not result in better performance [12,27].

The current injected from the source can be found by summing all the k-states and converting to an integral over energy as

$$I^+ = \frac{2q}{h} \int f_0(E, E_F) dE = q n_0 v^+. \tag{2.15}$$

For one dimensional transport the velocity and density of states cancels, which means the expression is independent of band structure. The solution to the integral can be expressed with help of the 0-order Fermi-Dirac integral as

$$I^+ = \frac{q k_B T_L}{\pi\hbar} \mathcal{F}_0(\eta_F), \tag{2.16}$$

with $\mathcal{F}_0(\eta_F) = ln(1 + e^{\eta_F})$. From equations 2.7 and 2.15 the electron velocity at the top of the barrier can be found as

$$v^+ = v_T \frac{\mathcal{F}_0(\eta_F)}{\mathcal{F}_{-1/2}(\eta_F)}, \tag{2.17}$$

where $v_T = \sqrt{2k_B T_L / \pi m^*}$. The quantity v^+ is also known as the injection velocity v_{inj}. This is an important parameter for devices operating close to the ballistic limit, more so than the electron mobility which will be discussed later. Similar equations can also be defined for the current injected from the drain, but with the energies related to the drain Fermi level by using $\eta_F - U_D$ instead of η_F. Finally, the net total current is

$$I = I^+ - I^- = \frac{2q k_B T_L}{h} \Big[\mathcal{F}_0(\eta_F) - \mathcal{F}_0(\eta_F - U_D) \Big]. \tag{2.18}$$

In summary, first the position of the top of the potential barrier is found by equations 2.5 and 2.12, which describes the balance between the gate potential and the mobile charges in the channel. When E_0 is known the current is readily available from equation 2.18. Some insights can be gained by analyzing the current expression under different constraints. In degenerate conditions where $\eta_F >> 1$ and $\mathcal{F}_0(\eta_F) \rightarrow \eta_F$ and with low drain bias the current can be approximated as

$$I = \frac{2q^2}{h} V_D. \tag{2.19}$$

Which shows that the conductance is quantized, each subband has a maximum conductivity of $2q^2/h$. Figure 2.3 shows the conductance steps for the three lowest subbands. Each subband will contribute with a conductance of $2q^2/h$. The distance between the steps depends on the quantization of the channel, with larger distance the smaller the channel dimensions. With high drain bias the current injected from the drain can be neglected and the total current is approximated to

$$I = \frac{2q^2}{h} \frac{E_{F,S} - E_0}{q}. \tag{2.20}$$

In degenerate conditions with high drain bias the electron concentration can be written as

$$n_0 = \frac{\sqrt{2m^*(E_{F,S} - E_0)}}{\pi\hbar}. \tag{2.21}$$

The electrostatic balance equation then becomes

$$\frac{E_{F,S} - E_0}{q} = (V_G - V_T) - \frac{q\sqrt{2m^*(E_{F,S} - E_0)}}{\pi\hbar C_{ox}}, \tag{2.22}$$

with $V_T = -E_{F,S}/q$. Using the quantum capacitance as in equation 2.14 the current in equation 2.20 can be written as,

$$I = \frac{2q^2}{h} \frac{C_{ox}}{C_{ox} + C_q} (V_G - V_T). \tag{2.23}$$

In the quantum capacitance limit where $C_{ox} >> C_q$, the current becomes $I = 2q^2(V_G - V_T)/h$, which gives a transconductance equal to the quantized quantum conductance. Therefore, what we should expect from a ballistic MOSFET in low temperature is that the low field conductance and the on-state transconductance to both be $2q^2/h$. In reality this is not the case since some scattering will occur in the channel, which will be discussed later but the ballistic modeling describes the upper limit of device performance.

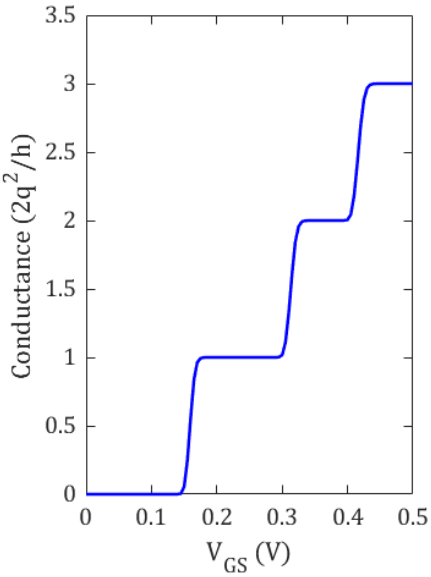

Figure 2.3: Simulated conductance of a 1D ballistic MOSFET, each subband will increase the conductance with $2q^2/h$.

2.3 GATE LEAKAGE

Classically there is no current going through the gate oxide, but as MOSFETs are scaled to smaller dimensions so is the thickness of the gate oxide, in order to keep proper electrostatic control of the channel. When the gate oxide is thin (generally a few nanometers) a tunnel current can occur [28–30]. It depends on the electron density in the channel n and the tunneling transmission probability T_t. The transmission probability can be approximated as [22]

$$T_t = e^{-2t_{ox}\sqrt{2m_{ox}(E_{C,ox}-E)}/\hbar}, \tag{2.24}$$

where t_{ox} is the gate oxide thickness, m_{ox} is the electron effective mass inside the oxide and $E_{C,ox}$ is the oxide conduction band position. The transmission probability has an exponential dependence on the oxide thickness but also reduces with a higher tunneling barrier.

2.4 NON-PARABOLICITY

In the effective mass approximation with parabolic bands the $E-k$ dispersion relation takes the form of,

$$E(k) = \frac{\hbar^2 k^2}{2m^*}. \tag{2.25}$$

This is only valid for small k-values, at higher applied biases electrons will occupy higher k-states where the approximation no longer is realistic. Using $\mathbf{k}\cdot\mathbf{p}$ theory this error can be diminished by introducing non-parabolic bands in the form of [3]

$$E(1+\alpha E) = \frac{\hbar^2 k^2}{2m^*}, \tag{2.26}$$

where the non-parabolicity factor α is material dependent constant and can be approximated as

$$\alpha = \frac{1}{E_g}\left(1-\frac{m^*}{m_0}\right)^2. \tag{2.27}$$

The subband energies can be found from 2.26 as

$$E_{n,m} = \frac{\gamma_{n,m}-1}{2\alpha}, \tag{2.28}$$

where

$$\gamma_{n,m} = \sqrt{1+\frac{2\alpha\pi^2\hbar^2}{m^\star}\left[\frac{n^2}{W_x^2}+\frac{m^2}{W_y^2}\right]} = \sqrt{1+4\alpha E_{n,m}^p} \tag{2.29}$$

This is under the assumption that the 1D channel is hard wall quantized in the x- and y-directions, setting the respective widths W_x and W_y. $E_{n,m}^p$ are the parabolic subband energies with subband index n and m. Comparing equation 2.26, 2.28 and 2.29, the subband effective mass will be adjusted by $m_{n,m}^* = m^*\gamma_{n,m}$ and the effective non-parabolicity factor by $\alpha_{n,m} = \alpha/\gamma_{n,m}$. The 1D density of states with parabolic bands for the lowest subband 2.6, will then be adjusted to

$$D_{1D}^{np}(E) = \frac{\sqrt{2m_{1,1}^*}(1+2\alpha_{1,1}(E-E_c))}{\pi\hbar\sqrt{(E-Ec)(1+\alpha_{1,1}(E-Ec))}}. \tag{2.30}$$

If $\alpha = 0$ this will reduce to the density of states with parabolic bands. The effect of the non-parabolicity is that density of states and effective mass increases at higher energies. The calculations become more cumbersome since the Fermi-Dirac integrals cannot be utilized and equation 2.5 have to be solved numerically.

2.5 OXIDE DEFECTS

Growing a high quality high-κ oxide on III-V semiconductors has proven to be a challenging task. Material defects in the oxide and in the semiconductor/oxide interface introduces energy states which can capture or emit electrons [31–33]. These traps can interact with the electrons in the semiconductor channel if the energy level of the traps is close to the semiconductor Fermi level. Traps situated in the conduction band can interact with mobile electrons in the channel during on-state operation, while traps in the band gap will impact the off-state performance. The traps can be divided into two groups, border traps which reside inside the gate oxide and interface traps which are at the semiconductor/oxide interface [34]. Border traps originate from disorder, oxide interstitials or vacancies a few atomic distances away from the interface. These traps can interact with the channel electrons via a tunneling process. Interface traps are associated with the non-ideal interface between the semiconductor and the oxide. Imperfections such as dangling bonds, faulty III-V bonds or oxygen vacancies will introduce a range of states distributed in energy, $D_{it}(E)$. During operation of the MOSFET these traps will be charged or uncharged depending on the gate voltage and their energy. A simple way to include this in the electrostatic model is to modify equation 2.12 to

$$E_0 = -qV_G + \frac{q^2(n_0 + n_{trap})}{C_G}, \tag{2.31}$$

with n_{trap} being the defect density at the top of the barrier. The current in equation 2.23 is then modified to be

$$I = \frac{2q^2}{h}\frac{C_{ox}(V_G - V_T)}{C_{ox} + C_q + q^2 D_{it}}. \tag{2.32}$$

Hence the traps can be included in the conduction model by adding an interface defect capacitance $C_{it} = q^2 D_{it}$, in parallel with C_q, as in figure 2.4. The interface defect density D_{it} is energy dependent and therefore gate voltage dependent but can as a first approximation be taken as a constant in the different regions of operation. The impact of the interface traps on the current is twofold. The first drawback can intuitively be understood by thinking of C_{it} as another capacitor that will be charged instead of introducing more electrons in the channel, which will in turn reduce the current through the device. The second implication is that the traps are static charges close to the channel. The conducting electrons will interact with the potential of the charged defects and scattering will increase. This leads to a reduced mean free path and electron mobility. The conclusion is that the interface between the

semiconductor channel and the insulating gate oxide is of great importance for MOSFET performance.

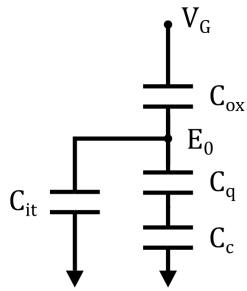

Figure 2.4: Capacative model of the MOSFET channel.

2.6 QUASI-BALLISTIC TRANSPORT

In a more realistic device, some scattering will occur within the channel, a scattering event will change the ***k***-vector and hence mixing of I^+ and I^- will take place. A simple way to include scattering in the ballistic model is to introduce the transmission coefficient T (where $0 < T < 1$), which describes the probability that an electron will be transmitted through the channel. Assume that under high drain bias some part of the ballistic current injected from the source will scatter in the opposite direction, this portion should then be included with the non-scattered current coming from the drain side as

$$I^- = TI_B^- + (1-T)I_B^+, \tag{2.33}$$

with the subscript indicating the fully ballistic current. The current can then be written as

$$I = T(I_B^+ - I_B^-) = TI_B. \tag{2.34}$$

Therefore, when scattering occurs and $T < 1$, the ballistic current will be reduced by the transmission coefficient. The transmission coefficient can be written as [35]

$$T = \frac{\lambda_0}{\lambda_0 + L_{eff}}, \tag{2.35}$$

where λ_0 is near equilibrium mean free path, L_{eff} is the effective gate length which is equal to the gate length at small drain bias and $L_{eff} = k_B T_L / qV_D$ at large drain bias. Large drain bias increases the transmission, since an electron scattering close to the drain is highly unlikely to return to the source again.

Scattering close to the drain has little effect on the drain current compared to scattering close to the source under high bias conditions [36, 37]. The mean free path is connected to electron mobility via the diffusion constant

$$D = \frac{\lambda_0 v_t}{2} = \frac{\mu k_B T_L}{q}. \tag{2.36}$$

Mobility is generally a concept used where the transport region is many mean free paths long. However, in short channel devices it is beneficial to instead think in terms of mean free path, where the probability to scatter in a distance dx is simply dx/λ_0. While the transmission coefficient provides a simple expression for the current, one should be aware that it also obscures some of the underlying physics.

2.7 SCATTERING THEORY

The electrons can move through a perfect lattice ballistically, but in a real crystal the electron will encounter some perturbation. Some different scattering mechanisms are shown in figure 2.5. The perturbations can be caused by defects, such as neutral impurities, dislocations and ionized impurities. Since the ionized impurities have a charge attributed to them, the scattering from this defect is stronger than from the other defects. In an alloyed crystal (such as InGaAs), variations in the composition will also introduce scattering. Carriers will interact with each other and produce scattering both from binary interaction between carriers and from interactions with plasmons (fluctuations in the carrier density). These effects can become important at high carrier densities. The presence of free carriers will impact the other scattering mechanisms by screening the perturbing potential. At room temperature, pertubations in the form of lattice vibrations are present.

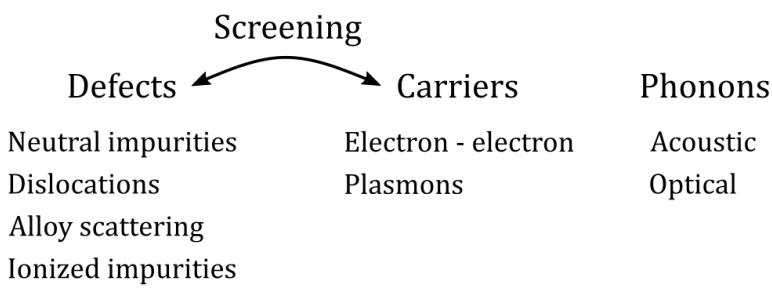

Figure 2.5: Overview of carrier scattering mechanisms.

These vibrational modes are described by phonon quasiparticles, this is often the dominating scattering mechanism except for at low temperatures where the phonon occupation is low. When an electron encounters a perturbation it will scatter, it will change from an original state $\boldsymbol{k}$ to new state $\boldsymbol{k}'$ [38, 39]. This process can happen through elastic scattering where the electron changes its momentum but not its energy. The electron can also experience inelastic scattering in which its energy is changed, this process is often mediated by a phonon. Scattering will greatly impact the electron transport and it can be described by a transition rate $S(\boldsymbol{k}, \boldsymbol{k}')$.

$$\begin{aligned} S(\boldsymbol{k}, \boldsymbol{k'}) = &\frac{2\pi}{\hbar} \left|H^a_{\boldsymbol{k'k}}\right|^2 \delta(E(\boldsymbol{k'}) - E(\boldsymbol{k}) - \hbar\omega) \\ &+ \frac{2\pi}{\hbar} \left|H^e_{\boldsymbol{k'k}}\right|^2 \delta(E(\boldsymbol{k'}) - E(\boldsymbol{k}) + \hbar\omega) \end{aligned} \tag{2.37}$$

This equation is known as Fermi's Golden Rule. The first term contributes when $E(\boldsymbol{k}') = E(\boldsymbol{k}) + \hbar\omega$, meaning that an energy of $\hbar\omega$ has been absorbed during the scattering event. The second term only contributes when $E(\boldsymbol{k}') = E(\boldsymbol{k}) - \hbar\omega$, resulting in the emission of energy $\hbar\omega$. The scattering matrix element $H_{k'k}$ describes the coupling between the initial and final state. It is written as

$$H_{k'k} = \frac{1}{\Omega} \int \Psi_{k'}(\boldsymbol{r}) U(\boldsymbol{r}) \Psi_k(\boldsymbol{r}) d^3\boldsymbol{r}, \tag{2.38}$$

where U is the scattering potential and Ψ is the real space wavefunction for the initial and final state.

The effects of scattering can be expressed in terms of a characteristic relaxation time τ, given by

$$\frac{1}{\tau(\boldsymbol{p})} = \sum_{\boldsymbol{p'}} S(\boldsymbol{p}, \boldsymbol{p'})[1 - f(\boldsymbol{p'})]. \tag{2.39}$$

This describes the rate at which a carriers with an initial momentum $\boldsymbol{p} = \hbar\boldsymbol{k}$ scatter to a state with momentum $\boldsymbol{p'} = \hbar\boldsymbol{k'}$, alternatively τ is the average time between scattering events. The factor $[1 - f(\boldsymbol{p}')]$ is the probability that the final state is unoccupied, in a non-degenerate semiconductor this factor can be approximated to 1. Figure 2.6 shows a schematic of a group of carriers injected with momentum $\boldsymbol{p}$ and its evolution in time. If the scattering mechanism is not isotropic, the direction of the final momentum will depend on the direction of the initial momentum. The momentum relaxation rate can be written as

$$\frac{1}{\tau_m(\boldsymbol{p})} = \sum_{\boldsymbol{p'}} S(\boldsymbol{p}, \boldsymbol{p'}) \left[1 - \frac{p'}{p} cos(\alpha)\right], \tag{2.40}$$

where α is angle between initial and final momentum. This describes the time required to completely randomize the momentum, which is possible to do with only elastic scattering, keeping the energy of the carriers unchanged. The energy relaxation rate is given by

$$\frac{1}{\tau_E(\boldsymbol{p})} = \sum_{\boldsymbol{p'}} S(\boldsymbol{p}, \boldsymbol{p'}) \left[1 - \frac{E(\boldsymbol{p'})}{E(\boldsymbol{p})} \right], \tag{2.41}$$

which takes the energy of the initial and final momentum into account. These characteristic relaxation times τ, τ_m and τ_E describe how the carriers are affected by scattering. The carrier mobility μ used in the MOSFET current equation is related to τ_m by

$$\mu = q \frac{\langle \tau_m \rangle}{m^*}. \tag{2.42}$$

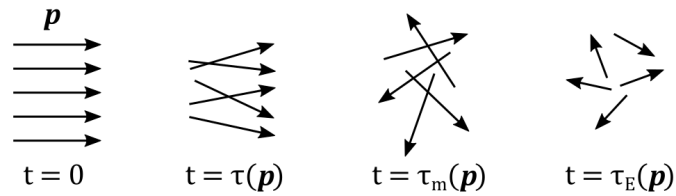

Figure 2.6: Schematic of how a group of carriers are affected by scattering and the related relaxation times.

The presence of free carriers will screen the scattering potential and reduce its effectiveness. This results in that electrons further away from a scattering potential will experience a screened potential instead and scatter less. Including screening, the momentum relaxation rate of electrons in a quantum well can be described by [40]

$$\frac{1}{\tau_m} = \frac{m^*}{2\pi\hbar^3 k_F^3} \int_0^{2k_F} \frac{|U(\bar{q})|^2}{\epsilon(\bar{q})} \frac{\bar{q}^2}{\sqrt{1 - \left(\frac{\bar{q}}{2k_F}\right)^2}} d\bar{q}. \tag{2.43}$$

$U(\bar{q})$ is the potential which is describing the scattering mechanism as a function of wave vector $\bar{q}$. The Fermi wave vector is given as $k_F = \sqrt{2\pi n_s}$, with n_s being the sheet electron density. The dielectric function of the two-dimensional electron gas is given as

$$\epsilon(\bar{q}) = 1 + V(\bar{q})[1 - G(\bar{q})]X^0(\bar{q}), \tag{2.44}$$

X^0 is the polarizability of the 2DEG given as 2D DOS. $G(\bar{q})$ is the Hubbard form of the local field correction [41]

$$G(\bar{q}) = \frac{1}{2g_v} \frac{\bar{q}}{\pi\sqrt{\bar{q}^2 + k_F^2}}, \tag{2.45}$$

with g_v being the number of degenerate energy bands. $V(\bar{q})$ is the electron-electron interaction potential and is given by

$$V(\bar{q}) = \frac{q^2}{2\epsilon_0\epsilon_s\bar{q}} F_C(\bar{q}), \tag{2.46}$$

with the form factor

$$F_C(\bar{q}) = \int |\Psi(z)|^2 dz \int |\Psi(z')|^2 e^{-\bar{q}|z-z'|} dz', \tag{2.47}$$

for electrons confined in the z-direction.

The mobility of a semiconductor depends on many different scattering mechanisms. Elastic scattering can occur from defects such as, neutral impurities, ionized impurities and dislocations. Since scattering from ionized impurities often is dominating, the other defect scattering sources are often ignored. For an alloyed semiconductor the variation in alloy composition will also generate scattering. In order to find the relaxation rate, the scattering potential $U(q)$ has to be identified for the different scattering mechanisms. For remote impurity scattering in a quantum well the potential can be written as

$$|U_R(\bar{q})|^2 = n_i \left(\frac{q^2}{2\epsilon_0\epsilon_s}\frac{1}{\bar{q}}\right)^2 F_R(\bar{q}, z_i)^2 \tag{2.48}$$

where n_i is the impurity sheet density concentration situated the distance z_i away from the quantum well. The form factor

$$F_R(\bar{q}, z_i) = \int |\Psi(z)|^2 e^{-\bar{q}|z-z_i|} dz \tag{2.49}$$

accounts for the distance between the impurity and the quantum well. In the presence of background doping in the quantum well the scattering is described by the potential

$$|U_B(\bar{q})|^2 = N_B a \left(\frac{q^2}{2\epsilon_0\epsilon_s}\frac{1}{\bar{q}}\right)^2 F_B(\bar{q})^2. \tag{2.50}$$

where N_B is the background doping density and

$$F_B(\bar{q}) = \frac{1}{a} \int F_R(\bar{q}, z_i) dz_i, \tag{2.51}$$

with a as the thickness of the quantum well. In an alloy semiconductor, for example InGaAs where there is intermixing of indium and gallium, will lead to alloy scattering described by an average scattering potential [42]

$$|U_A|^2 = \frac{3x(1-x)V_a^2\Omega_A}{2a}. \tag{2.52}$$

This is under the assumption that it is a perfectly random alloy. The scattering potential depends on the alloy composition x and $\Omega_A = \sqrt{3}\pi a_L^3/16$, with a_L being the lattice constant. By inserting the respective scattering potential in equation 2.43, the momentum relaxation rate for that scattering process can be found.

Inelastic scattering occurs from a from a scattering potential varying in time, most commonly from lattice vibrations. The vibrational modes in the crystal are often described in terms of phonon quasiparticles. Acoustic phonons are similar to sound waves where the atoms move in the same directions as their neighbors during the vibrations. This scattering is also known as acoustic deformation potential scattering since the phonon compresses and dilates the crystal at different points. Optical phonons are a vibrational mode where the atoms in the unit cell move in opposite directions, if the atoms have slightly different charge (as in InGaAs) this will induce an electric field which will scatter the carriers. This polar optical phonon scattering is often the dominating scattering mechanism at room temperature. The relaxation rate due to polar optical phonon scattering in a quantum well, with bulk phonons and only the first subband considered can be written as [43, 44]

$$\frac{1}{\tau_{pop}^A} = \frac{e^2\omega_0 N_0 m^* a}{8\pi^2\hbar^2\epsilon_0\epsilon_p} \times \frac{1 - f_0(E_F + \hbar\omega_0)}{1 - f_0(E_F)} \tag{2.53}$$

for phonon absorption and

$$\frac{1}{\tau_{pop}^E} = \frac{e^2\omega_0(N_0+1)m^*}{a\hbar^2 k_F^2\epsilon_0\epsilon_p} \times \frac{1 - f_0(E_F - \hbar\omega_0)}{1 - f_0(E_F)} \tag{2.54}$$

for phonon emission. $N_0 = e^{\hbar\omega_0/k_B T_L} - 1$ is the phonon occupation number, ω_0 is the optical phonon frequency, a is the thickness of the quantum well and $\epsilon_p = 1/(\frac{1}{\epsilon_\infty} - \frac{1}{\epsilon_s})$, where ϵ_∞ and ϵ_s is the high frequency and static dielectric constant respectively. The last factor utilizes the Fermi-Dirac distribution to consider the occupation (or lack thereof) of the initial and final scattering state. The acoustic phonon deformation potential relaxation rate is written as [45]

$$\frac{1}{\tau_{adp}} = \frac{3m^* D_A^2 k_B T_L}{2\hbar^3\rho v_s^2 a}. \tag{2.55}$$

Apart from the quantum well thickness it also depends on the deformation potential amplitude D_A, the mass density ρ and the sound velocity in the semiconductor v_s.

Using Matthiessen's rule and equation 2.42 the total effective mobility can be written as

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{pop}} + \frac{1}{\mu_{adp}} + \frac{1}{\mu_{bg}} + \frac{1}{\mu_{alloy}} + \frac{1}{\mu_{imp}} \tag{2.56}$$

An example of a mobility calculation can be seen in figure 2.7, each mobility component can be seen together with the total effective mobility. The scattering process with the highest momentum relaxation rate will basically determine the effective mobility.

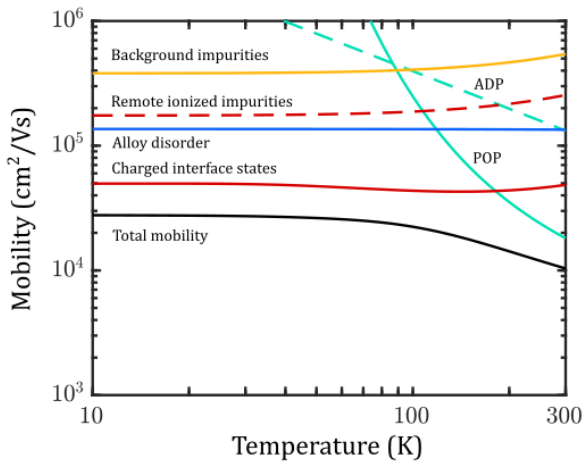

Figure 2.7: Mobility components and effective mobility as a function of temperature. In this case the scattering from ionized impurities has been divided in to two groups, scattering from defects at the quantum well interface and scattering from remote ionized impurities.

2.8 LOW TEMPERATURE TRANSPORT AND BAND TAILS

Disorder in the semiconductor crystal such as crystalline disorder, impurity disorder, surface roughness and strain, lead to the formation of band tail states. These states are situated just above the valence band edge or just below the conduction band edge and display an exponential distribution in energy defined by a characteristic Urbach energy [46–48]. The density of the

band tail states can be written as

$$D_T = N_{2D} e^{((E-E_c)/E_u)}, E < E_c, \tag{2.57}$$

where the Urbach energy E_u determines the exponential fall off further from the band edge. Including the density of the band tails with the standard DOS above the band edge will basically extend the density of states inside the band gap. This will impact the transport in the MOSFET channel below V_T, deteriorating the subthreshold swing. An empirical expression of the density of states can be formulated. Here, given for 2D quantization and including non-parabolicity

$$D_{2D}(E) = \frac{m^*}{\pi\hbar^2}\left[\mathcal{F}_{-1}\left(\frac{E-E_c}{E_u}\right) + 2\alpha E_u \mathcal{F}_0\left(\frac{E-E_c}{E_u}\right)\right], \tag{2.58}$$

utilizing the generalized Fermi-Dirac integrals. The parabolic, non-parabolic and DOS including band tails are shown in figure 2.8. The band tails will broaden the band edge and introduce states below E_c.

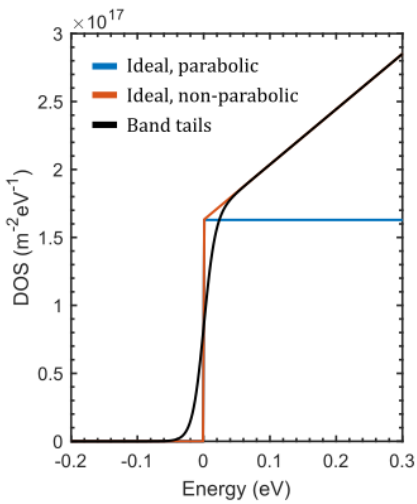

Figure 2.8: DOS for parabolic and non-parabolic bands. As well as DOS including the band tail states, which broadens the band edge and introduces states below $E_c = 0$.

Understanding of the effects of the band tails are especially important for MOSFETs operating at cryogenic temperatures. The inverse subthreshold

slope of a MOSFET can be written as

$$S = ln(10)\frac{k_B T_L}{q}\left(1 + \frac{C_q + C_{it}}{C_{ox}}\right). \tag{2.59}$$

With small C_q and C_{it} this approaches the Boltzmann limit of 60 mV/dec at room temperature. However, for small temperatures this expression predicts very small inverse subthreshold slopes (0 mV/dec at 0 K). Experimental device data often shows much larger values, in the range of 10 – 30 mV/dec [49–51]. The discrepancy can be compensated with an increased D_{it} close to the band edges with lower temperatures, but this often result in unreasonable high estimate of D_{it}. Instead, using the band tail approach can explain the saturation of the inverse subthreshold slope at low temperatures. Due to band tails the inverse subthreshold slope will saturate below a critical temperature $T_0 = E_u/k_B$, according to

$$S = ln(10)\frac{k_B T_0}{q}\left(1 + \frac{C_q + C_{it}}{C_{ox}}\right). \tag{2.60}$$

Another aspect of electron transport through a MOSFET channel at cryogenic temperatures, is the roughening of the conduction band edge due to charged defects in the oxide or at the semiconductor/oxide interface [52]. The change in the energy landscape is illustrated in figure 2.9(a), with large enough potential fluctuations this can be thought as of a chain of quantum dots along the channel. This leads to the possibility of electron transport through the channel below E_c due to sequential tunneling through the available states, which gives rise to peaks in the current at low drain bias. At higher temperatures or larger drain biases the peaks are broadened. The roughening of the conduction band edge can be reduced by either reducing the charged defect concentration by improving the semiconductor/oxide interface or by moving the interface away from the conducting electrons. A simulated conductance of a MOSFET with a rough conduction band edge at low temperatures is shown in figure 2.9(b). The current is calculated by a 1D real space tight-binding non equilibrium Green's function (NEGF) model. The transmission and resonance peaks are highly dependent on the exact potential variation along the channel. The transport properties in subthreshold of a MOSFET at cryogenic temperatures is determined by the band tail parameter E_u and the density of the interface traps D_{it}.

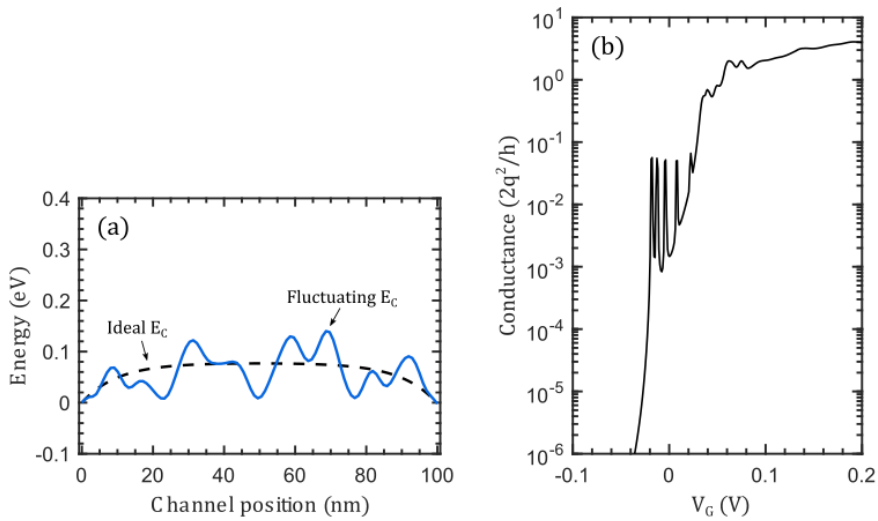

Figure 2.9: (a) Schematic of potential fluctuations of E_c along the channel length. (b) Simulated conductance at 40 mK using a 1D real space tight-binding non equilibrium Green's function (NEGF) model. Clear conductance resonance peaks can be seen.

2.9 HALL EFFECT MEASUREMENTS

Hall effect measurement is a well-established technique to determine the carrier concentration, carrier type and carrier mobility in a thin film. It is based on the Hall effect discovered by Edwin Hall in 1879. A charge carrier with charge q will experience forces both from an electric field and a magnetic field as [39]

$$F = q\boldsymbol{E} + q\boldsymbol{v} \times \boldsymbol{B}. \tag{2.61}$$

The last term is the Lorentz force which is perpendicular to the velocity $\boldsymbol{v}$ and the magnetic field $\boldsymbol{B}$. The Hall effect measurement technique exploits this phenomenon to be able to extract the density of the charge carriers. This can be done by creating a test setup such as in figure 2.10, where a current I is sourced through a long and thin sample with thickness t, and width w. The contacts are designed such as the current only flows in the positive x-direction. A magnetic field is then applied in the z-direction and the Lorentz force will make the charge carrier rotate around the B-field lines (in the xy-plane) with a certain cyclotron frequency given by $f = qB_z/2m$ and radius, $r = mv/qB_z$ where m is the mass of the charge carrier. Since no current can escape the sample in the y-direction, charge will be accumulated on one side

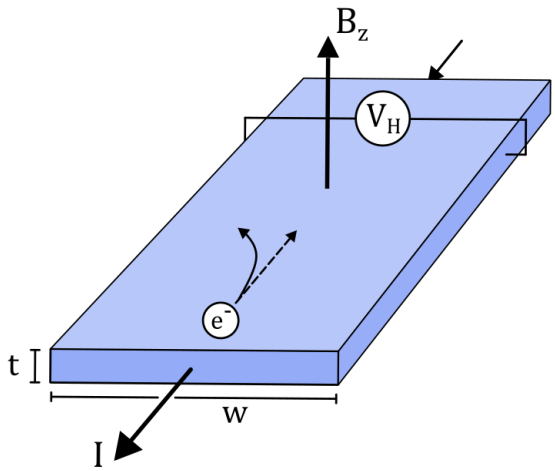

Figure 2.10: Schematic figure of a Hall voltage measurement. The Lorentz force will change the electrons path which result in an accumulation of charge on one side of the sample. This potential is measured as the Hall voltage, V_H.

of the sample and depleted on the other. This is introducing an electric field in the y-direction (V_H/w) which at steady state will be equal and opposite the Lorentz force. This leads to the equality,

$$\frac{qV_H}{w} = qv_xB_z, \tag{2.62}$$

and with the charge carrier velocity $v_x = I/qnwt$ this can be rearranged to give

$$n = \frac{IB_z}{qV_Ht}. \tag{2.63}$$

Therefore, by measuring the Hall voltage V_H across the sample the charged carrier type and density can be extracted. Note that only moving charges which are a part of the current will impact the Hall voltage, for example charged defects on the sample surface are fixed and will not be included in a Hall measurement. This is in contrast to capacitive measurement where fixed charges will be included assuming they are in the appropriate energy range and time scale.

In order to determine the charge carrier mobility, the sample resistivity also have to be characterized. A common measurement scheme for resistivity measurements is the van der Pauw technique [53], which is able to determine the resistivity of arbitrarily shaped geometries. The sample must be uniform

and without holes in the conducting layer. The contacts should be placed at the perimeter of the sample as in figure 2.11. By sourcing a current through contacts 1 and 2 while measuring the voltage drop between contacts 3 and 4 a resistance $R_{12,43} = V_{43}/I_{12}$ can be determined. Repeating this measurement by sourcing current along one edge of the sample and measure the voltage drop on the opposite edge of the sample, two characteristic resistances can be determined, $R_{vertical} = (R_{12,43} + R_{43,12})/2$ and $R_{horizontal} = (R_{23,14} + R_{14,23})/2$. The van der Pauw equation

$$1 = e^{(-\pi R_{vertical}/R_s)} + e^{(-\pi R_{horizontal}/R_s)}, \tag{2.64}$$

is then solved numerically to find the sheet resistance R_s. The sample resistivity is then $\rho = R_s t$. With the carrier concentration and the resistivity known the carrier Hall mobility is then given by

$$\mu_{Hall} = \frac{1}{\rho n q}. \tag{2.65}$$

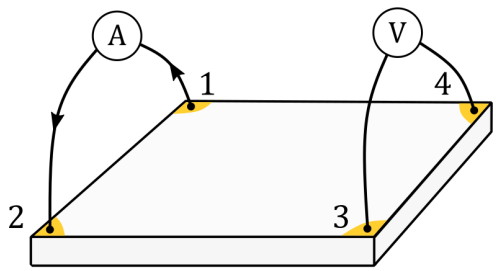

Figure 2.11: Schematic of a rectangular geometry prepared for resistivity measurements.

3

MOSFET Fabrication

Throughout this project a variety of different device structures have been fabricated, utilizing common semiconductor fabrication techniques such as, metal organic vapor phase epitaxy (MOVPE), electron beam lithography (EBL), metal evaporation, atomic layer deposition (ALD) and more. In this section, some of the important steps will be underlined together with some process considerations. In appendix A a more detailed description of the fabrication process is given.

3.1 NANOWIRE AND CONTACT GROWTH

In this project, the metal organic vapor phase epitaxy (MOVPE) technique has been used to grow lateral nanowires. MOVPE is an established chemical vapor deposition (CVD) technique with large industrial application. The growth process is based on a laminar flow of precursors molecules which enter a heated reactor where they undergo reactions in both the vapor phase and on the sample surface to form the semiconductor crystal [54, 55]. To limit the vapor phase reaction rate, the process is often performed at reduced pressure, typically 100 mbar. Close to or at the heated sample surface, the precursor molecules will decompose through several reaction steps. The metal organic precursors often come in the form of MR_n, where M is the element forming the crystal and R_n is an alkyl such as methyl CH_3. The precursors have to fulfill some requirements, they need to have low stability in order to decompose in the reaction process. It is also favorable if they can be stored as a liquid with high vapor pressure, since this enables a more stable flow of molecules into the reactor. Suitable precursor can be designed to fulfill

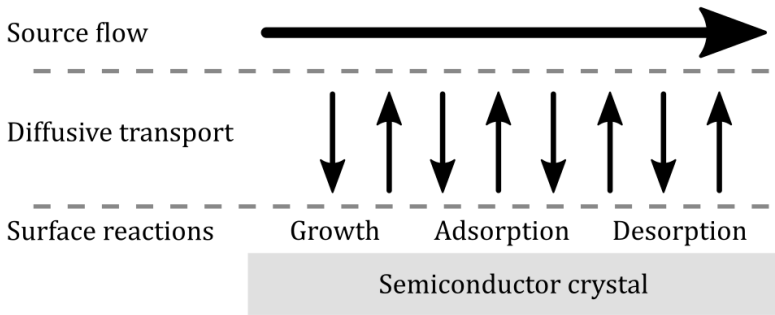

Figure 3.1: Overview of the different processes involved in MOVPE.

the requirements for MOVPE since the metal-carbon bond is dependent on the electronegativity of *M* and the size and configuration of the ligand *R*. Usually the bond strength decreases as number of carbon atoms that bond to the central carbon in the alkyl is increased.

MOVPE is a highly non-equilibrium process where the driving force is given by the drop in chemical potential from the input gas phase to the solid crystal. Figure 3.1 summaries the growth steps, the laminar flow of carrier gas and source molecules supplies the reaction. Some distance above the sample surface there is a vertical diffusive transport layer originating from reactions from source molecules and incorporation in the crystal. At the surface there are adsorption/desorption of molecules and as well as incorporation of atoms in the crystal lattice. The complete successive chain of reactions will be limited by the slowest process. If the input flow of source molecules and the output flow of waste molecules is high enough, the growth process will be limited by the reaction rate. This is called the kinetically limited growth regime, since the reactions are limited by some activation energy, the growth rate will be dependent on the temperature. If instead the growth reaction rate is much faster than the rate that the source molecules can arrive at the interface, the growth is said to be in the transport limited regime. Since gas phase diffusion only weakly depends on the temperature, this regime is nearly temperature independent. MOVPE is usually performed in the transport-limited regime where the exact sample surface temperature has a weak effect on the growth rate, crystal composition and doping levels. In growth of III-V semiconductors the group V precursors are often more volatile than the group III precursors. This means that the growth is often performed with the partial pressure $P_V >> P_{III}$ in the vapor phase. But at the growth interface both group III atoms and group V atoms are incorporated into the crystal with the same rate

leading to almost complete depletion of group III at the interface. This means the growth rate is controlled by the supply of group III atoms at the growth interface.

The lateral nanowires in this project have been formed using selective area growth (SAG) of InGaAs on an (100) InP:Fe semi-insulating substrate. SAG is a technique where a mask blocks the growth on certain areas on the substrate. The advantage of this method is that it is catalyst free and offers a great degree of freedom in the design of the growth mask. Since the growth mask is designed in a lithography step, the control of the size, position and pitch is set by the lithography system. This is under the assumption that the growth process is designed in such a way that the lateral growth direction is much slower than the vertical, which limits mask overgrowth. It is relatively trivial to construct connected lateral nanowires or even networks of nanowires in a single growth step. This is an important property for large scale fabrication. Another approach to form lateral nanowires is to etch out the nanowires from a thin film, but this might lead to damage on the crystal surface from the etching process. One of the drawbacks of lateral nanowires compared to a vertical structure is the difficulty to grow a heterostructure in the electron transport direction. This often leads to a need of a second growth step to create highly doped n^+ contacts. However, the bottom-up process used in this project enables the formation of lateral nanowires with clear facets with great size control and positional alignment.

Hydrogen silsequixane (HSQ) has been used as a growth mask, this is a flowable oxide resist which transforms into SiO_x-like structure when exposed to an electron beam. Figure 3.2 shows a schematic of the nanowire fabrication steps. First the HSQ is patterned by EBL where the openings in the HSQ will set the width of the grown nanowires. When creating small feature sizes (few

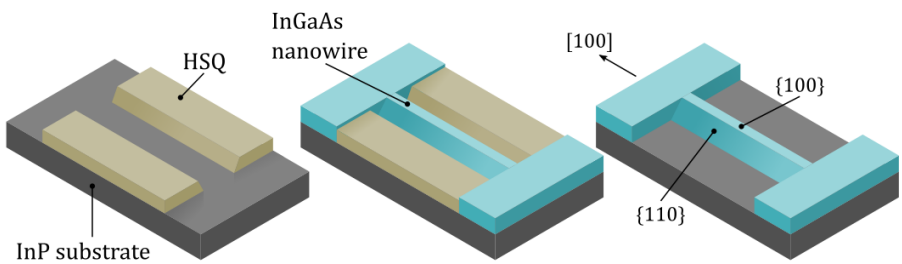

Figure 3.2: Schematic of the selective area growth of lateral nanowires. HSQ is patterned as a growth mask, the growth will be inhibited on the HSQ areas. After this, the InGaAs layer is grown by MOVPE. Finally, the HSQ mask is removed, leaving a lateral nanowire.

tenths of nanometers) the contrast of the lithography process is important, but so is the adhesion. The HSQ adhesion to the InP substrate can be improved with proper oxidation of the surface before resist spinning and with a higher pre-exposure baking temperature. The increased baking temperature will result in a reduced contrast ratio. Therefore, there is a trade of to be considered between adhesion and contrast. The contrast can be improved by resist development at elevated temperatures, in this project the majority of the samples were developed in trimethylammonium hydroxide (TMAH) at 40 °C. Just before the sample is loaded into the MOVPE reactor it is cleaned in diluted hydrogen flouride (HF) to remove native oxides. The cleaning of the sample surface is critical to minimize the defect density at beginning of the growth. The resulting facets of the grown nanowire is dependent on the substrate orientation and the orientation of the mask openings. The mask alignment most commonly used in this project gives a nanowire with (100) top facet and {110} side facets. These facets grow away from the mask, limiting the mask overgrowth.

The growth is done in a horizontal reactor at a pressure of 100 mbar with H2 as the carrier gas. At the beginning of the growth process the sample is heated to a high temperature under phosphine (PH_3) pressure, this is done to allow desorption of native oxides. The growth step is done at 600 °C, it starts with a few nanometers of InP growth followed by 13 nm InGaAs growth. The precursors used are trimethyl indium (TMIn), trimethyl gallium (TMGa), and arsine (AsH_3). The $In_xGa_{1-x}As$ growth rate is 0.5 nm/s. The sample is then cooled under AsH_3 pressure to prevent As desorption. The resulting thin film $In_xGa_{1-x}As$ has a composition with x = 0.65. Due to the presence of the mask, the composition of the nanowires have an increased indium content compared to the thin film layer away from the mask areas [56]. The sticking coefficient and the mean free path of the adatom on the surface is surface dependent, this might lead to a situation where the concentration of indium on the mask surface is increased compared to the concentration of indium adatoms on the semiconductor surface. After the growth, the HSQ is stripped by a buffered oxide etch (BOE), note that this will also remove the native oxides on the semiconductor surface.

In order to create an ohmic contact between the semiconductor and metal, highly doped n^+ contact regions are grown. The doping precursor used is tetraethyltin (TESn) which has a high solubility in InGaAs. The doping precursor flow during the growth is calibrated in such a way that the doping concentration is maximized without leaving excess tin droplets on the surface. This minimizes the contact resistance and the sheet resistance of the layer. The growth of 30 nm $In_{0.63}Ga_{0.37}As$ with a doping concentration of $5 \cdot 10^{19}$ cm^{-3} is done at 600 °C. Apart from the doping, the indium content also

impacts the contact resistance, generally the higher indium content the better contact [57, 58]. Some considerations have to be made regarding the InGaAs composition compared to the layer thickness. If the n^+ contact layer is grown to thick, the layer might relax due to the lattice mismatch to the channel and substrate. During the growth, the channel area is masked by using a HSQ dummy gate, the gate length of the device is the determined by the width of the dummy gate. Aligning the dummy gate as in figure 3.3 will create {111}B facets sloping away from the channel area.

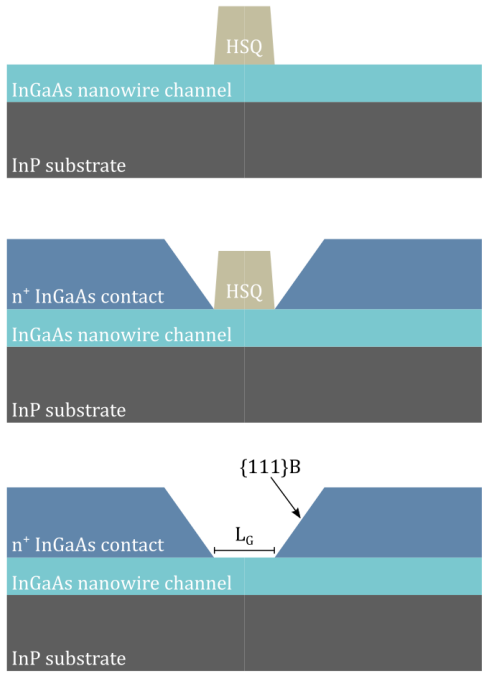

Figure 3.3: Schematic of the selective are growth of n^+ contacts. A HSQ dummy gate is patterned as a growth mask along [110], protecting the channel area. After this, the n^+ InGaAs layer is grown. Finally, the HSQ mask is stripped.

3.2 MESA DEFINITION

At this stage in the fabrication process the majority of the sample surface is InGaAs which is conducting, which means that the devices have to be electrically separated from each other. This is done by masking the active

device areas before performing a wet etch in H_3PO_4:H_2O_2:H_2O (1:1:25), which has an InGaAs etch rate of roughly 2 nm/s, but will not etch InP. The etch time has to be set according to the thickness of the grown InGaAs layers, both the nanowire growth and the contact growth. Since the InP will act as an etch stop layer there is generally no issues with over etching the InGaAs as long as mask adhesion is good. Next, 16 nm of the InP substrate is etched by HCl:H_2O (1:1) with an etch rate of approximately 4 nm/s. The InGaAs etch is isotropic though it relies on oxidation of the InGaAs by the H_2O_2 and then the oxides are removed by the H_3PO_4. The InP etch is anisotropic with a high etch rate on some facets, namely (100) and (110) while (111B) is etched slowly [59]. The etch mask used has either been EBL defined HSQ or UV defined S18 resist depending on the resolution and alignment requirements. When using HSQ as an etch mask there is an added opportunity to deposit a dielectric layer which will isolate the pads from the substrate. Before removal of the HSQ, a deposition of roughly 14 nm of SiN_x using plasma-enhanced chemical vapor deposition (PECVD) is performed. Removing the HSQ by BOE will leave the SiN_x layer everywhere on the sample surface except on the mesa. Figure 3.4 is a SEM image showing a device after the mesa step.

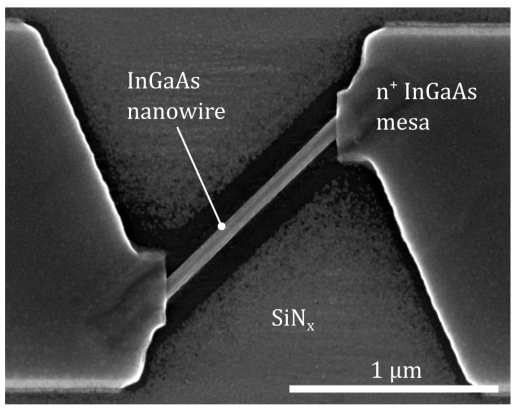

Figure 3.4: SEM image of a nanowire device. The SiN_x is covering the sample surface except on the nanowire and the mesa .

3.3 DIGITAL ETCHING

Digital etching is a process used for removing a small amount of material from top surface of the sample in a very controlled manner. This is used to reduce the dimensions of the nanowire, it also has the added benefit of cleaning the

sample surface. Each digital etch cycle consists of sample oxidation by ozone followed by a removal of the formed oxide in diluted HCl. The oxidation process is self-limiting since after the initial oxide is formed, to continue the oxidation the ozone must diffuse through the already formed oxide, which significantly slows down the oxidation rate. Each cycle will remove 1.4 nm of InGaAs.

3.4 SOURCE AND DRAIN METALLIZATION

In this project, the most commonly used metal stack is Ti/Pd/Au, which has been shown to form a good ohmic contact with InGaAs [60, 61]. Titanium has good adhesion to III-V semiconductors and the palladium is a diffusion barrier to prevent gold from entering the semiconductor contact during annealing. The lithography was done using PMMA exposed in EBL or UV exposed ma-N depending on resolution and alignment requirements. Just prior to metal evaporation the sample is submerged in diluted HCl in order to remove native oxides. Figure 3.5 shows the device structure after metal evaporation and lift-off.

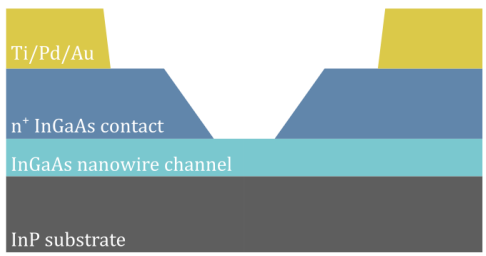

Figure 3.5: Schematic of the device structure after contact metallization lift-off process and resist stripping.

3.5 GATE FORMATION

First the insulating gate oxide has to be deposited, this is a critical step for the device performance. To limit the interface trap density and minimize oxide defect states the number of dangling bonds present at the InGaAs surface should be minimized. This done by passivation in 10 % ammonium sulfide solution for 20 minutes just before the sample is placed in ALD chamber [62]. The initial steps of the ALD process is an in-situ surface cleaning by a few

cycles of trimethyl aluminum (TMAl) which is known to reduce interface traps by removing the native oxide [63]. In this project the most commonly used gate oxide is a bilayer of Al_2O_3 and HfO_2. The Al_2O_3 deposited at a temperature of 300 °C is known to create a good interface with InGaAs, and the HfO_2 deposited at 120 °C, has a high dielectric constant and low leakage. The deposited Al_2O_3 is usually less than 1 nm thick. The high dielectric constant of HfO_2 is important to maintain a high gate-channel capacitance even when a thicker gate oxide is used to minimize leakage currents. The deposited HfO_2 is usually a few nanometers thick, but can be varied depending on if gate leakage or gate capacitance is prioritized. Finally, the gate metal Ti/Pd/Au is deposited using a lift of process using either PMMA exposed in EBL or UV exposed ma-N.

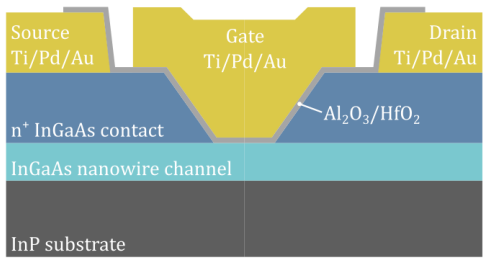

Figure 3.6: Schematic of the final device structure.

4

Device Characterization

During this project the fabricated InGaAs nanowire and quantum well devices have been characterized by mainly using three measurement techniques I-V measurements, Hall measurements and C-V measurements.

4.1 NEAR SURFACE QUANTUM WELLS AND NANOWIRES

In paper I, Hall measurements were extensively used to study the electron mobility of near surface InGaAs/InP quantum well layers. Extracted electron concentration, mobility and resistivity were compared with scattering simulations to quantify the surface charge defect density. Mobility measurements on both surface quantum wells and on buried quantum wells are presented in figure 4.1. The structure in (a) consists of a 13 nm InGaAs channel buried below a 25 nm InP top barrier. The channel has a 4 nm thick Si-doped layer situated 4 nm from the channel on both sides. The structure in (b) doesn't have the InP top barrier so the InGaAs quantum well is situated directly at the surface. The mobility of both structures is limited by scattering due to charged interface states. The buried quantum well exhibits a mobility of 27800 cm^2/Vs at 10 K while the surface quantum well has a mobility of 4000 cm^2/Vs. This is due to that when the charged interface states are moved away from the conducting electrons in the InGaAs layer, the scattering rate will decrease. This effect can make it challenging to fabricate surface quantum wells with very high mobilities, an exceptional surface with very low defect density is required. On the other hand, the advantage of the higher mobility of a buried quantum well can be utilized in a RF MOSFET spacer region reducing the access resistance. The development of the modulation doped layers was also utilized for the RF MOSFETs in paper V. Hall measurements

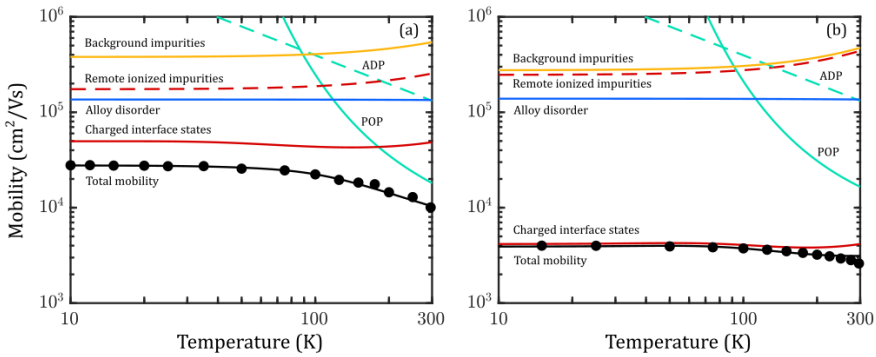

Figure 4.1: [64] Calculated mobility components and effective mobility as a function of temperature together with measured data (circles). (a) Buried quantum well with 25 nm InP top barrier. (b) Surface quantum well passivated by Al_2O_3/HfO_2.

are also a great characterization technique to utilize when developing and fine-tuning semiconductor MOVPE growth recipes, since it can be used to determine the carrier concentration and mobility of the grown layers. After growth, it is quick to process the samples to be ready for Hall measurements, only some metal contacts have to be deposited (which for a planar layer can be done without resist, using a shadow mask).

In paper II, the band structure properties of strained InGaAs quantum wells on InP were modeled by an eight band **k**·**p** theory. Band structure parameters are calculated for thin quantum wells (~10 nm). As expected, the $In_xGa_{1-x}As$ bandgap and effective mass shifts when including the strain in the model. The unstrained and strained calculations give the same values for composition x = 0.53, when $In_xGa_{1-x}As$ is lattice matched to InP. For compositions x > 0.53 the bi-axial compressive strain increases the bandgap and the effective mass compared to an unstrained quantum well with the same thickness. The bandgap and effective mass instead decrease for compositions x < 0.53 when there is tensile strain. Large planar InGaAs quantum well MOSFETs were fabricated and characterized by I-V, C-V and Hall measurements. An electrostatic model including non-parabolicity, band tails, and interface traps was able to accurately fit the measured data at both 13 K and 300 K. Some measured data together with the fitted model is shown in figure 4.2.

The surface conditions of the InP are very important for the quality of the grown InGaAs layer, especially for thin quantum wells. This was investigated in paper III by fabricating long channel InGaAs quantum well MOSFETs with different pre-treatment prior to the MOVPE growth step. The growth

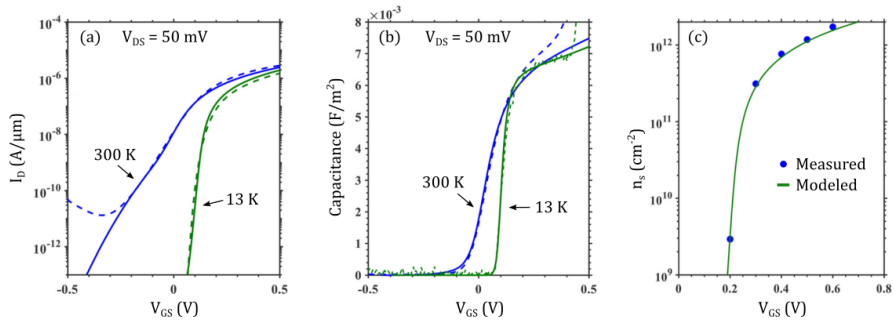

Figure 4.2: [65] (a) Measured (dash line) and modeled (solid line) transfer characteristics of an InGaAs MOSFET with $W_G = 70$ μm and $L_G = 6$ μm. (b) Measured (dashed line) and modeled (solid line) low frequency capacitance as a function of gate voltage. (c) Measured and modeled sheet carrier density.

was confirmed to be in step-flow growth mode by examine the surface of the InGaAs by using atomic force microscopy (AFM). Donor like defects at the InP/InGaAs forming at the initial steps of the growth deteriorates the gate modulation and off-state performance. All devices were characterized by I-V measurements at room temperature and some at 13 K. Extracted inverse subthreshold slope was the main metric comparing the different pre-treatments. The most suitable pre-treatment of the ones tested was a short clean in diluted HF, which is also compatible with the HSQ mask process used for the selective area grown nanowires.

In paper XIII the surface off selective are grown InGaAs nanowires were investigated by scanning tunneling microscopy and spectroscopy (STM/S). Figure 4.3(a) shows a STM topography images of several nanowires close to each other, similar to the design used in paper V. The nanowires were confirmed to have a top facet of (001) with a 4×2 surface reconstruction and a root mean square roughness of 0.12 nm. This indicates that it is possible to achieve a well-ordered surface after atomic hydrogen cleaning. This is promising for the prospect of using in-situ atomic hydrogen annealing as pre-cleaning step for either gate oxide deposition or contact metallization. Variations of the band gap along the nanowire was investigated by acquiring STS point spectra at several positions along the nanowire, seen in figure 4.3(b). The band gap at position 4 on the planar area next to the nanowires has a measured band gap of 490 meV. The band gap is decreasing towards the middle of the nanowire, with values of 410, 420 and 440 meV at positions 1, 2 and 3 respectively. This indicates an increase of the indium content towards

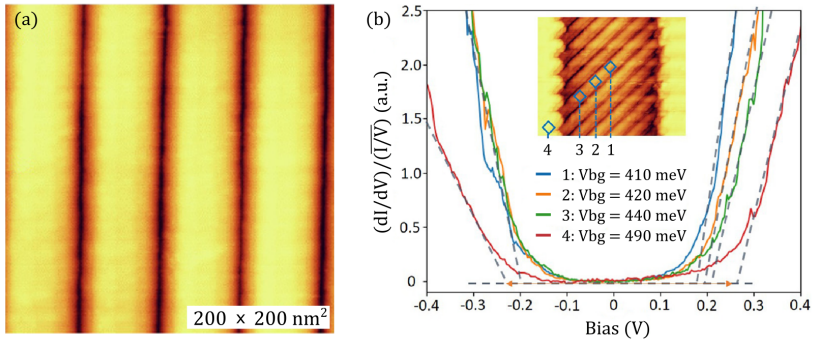

Figure 4.3: [66] (a) STM topography image of several nanowires, the scanned area is 200×200 nm^2. (b) Averaged $(\partial I/\partial V)/(\overline{I/V})$ spectra at position 1-4, as seen in the inset. The dashed lines are fitted to the valence band and conduction band onset.

the center of the nanowires, which is beneficial for MOSFETs due to generally higher electron mobility.

4.2 III-V MOSFETS FOR HIGH-FREQUENCY APPLICATIONS

MOSFETs for high-frequency application have been fabricated by building on the knowledge from the DC process. Paper IV and V include MOSFETs with two different approaches to constructing suitable spacers for low capacitance high-frequency operation. The design in paper IV is a planar InGaAs quantum well MOSFET utilizing a self-aligned sacrificial amorphous Si spacer, to achieve parasitic capacitances comparable to state-of-the-art HEMTs. The capacitances are extracted from measured S-parameters and their scaling behavior with device dimensions are investigated. The device layout and capacitances can be seen in figure 4.4. The total device capacitance is divided into intrinsic capacitance $C_{gg,i}$ and parasitic capacitance $C_{gg,p}$. The parasitic capacitance is identified by two parts. The extrinsic parasitic capacitance $C_{gg,ep}$ which is a fixed capacitance originating from the non-de-embedded contacts routing and the intrinsic parasitic capacitance which scales with the gate width. The total gate capacitance can be written as $C_{gg} = C_{gg,ep} + C_{gg,ip}W_G + C_{gg,i}W_G L_G$. Figure 4.5 shows the extracted capacitances. The parasitic capacitance was extracted in the off-state where the intrinsic capacitance is negligible. The smallest parasitic capacitance achieved were $C_{gs,ip} = 0.22$ fF/µm and $C_{gd,ip} = 0.25$ fF/µm. The main contribution to the intrinsic parasitic capacitance comes from the gate overlap of the n$^+$ contacts.

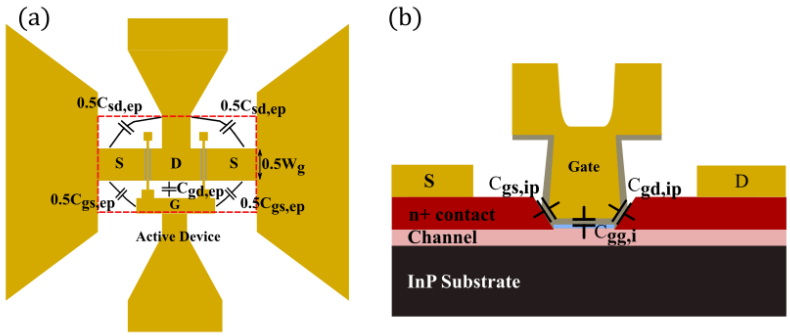

Figure 4.4: [67] (a) Device contacts and pad layout, including extrinsic capacitances. The red dashed line is the reference plane. (b) Device cross-section illustrating the intrinsic and intrinsic parasitic capacitances.

The mean overlap is estimated to be 3.5 nm on the source and 5 nm on the drain. It is important to minimize this overlap, this requires extremely accurate alignment or preferably a self-aligned process. The intrinsic capacitances in triode (saturation) is $C_{gs,i} = 0.39$ µF/cm^2 ($C_{gs,i} = 0.38$ µF/cm^2) and $C_{gd,i} = 0.31$ µF/cm^2 ($C_{gd,i} = 0.02$ µF/cm^2).

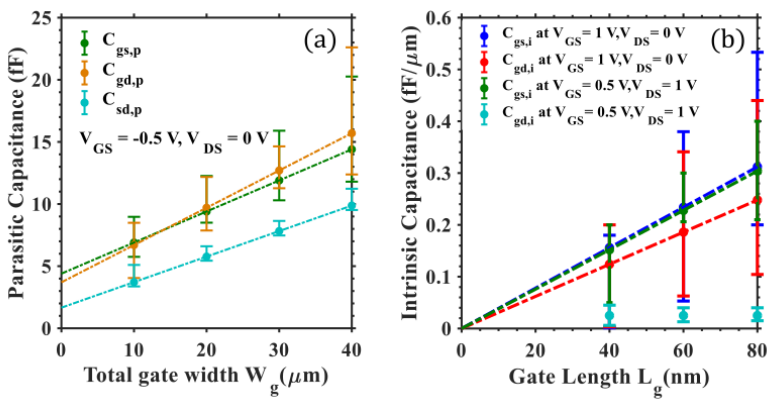

Figure 4.5: [67] (a) Parasitic capacitances as a function of total gate width together with linear fit (dashed line). (b) Intrinsic capacitances normalized to gate width as a function of gate length. The dashed lines are linear fits to the respective capacitance.

The device of paper V are based on hundreds of nanowires horizontally stacked close to each other. The MOSFET structure is shown in figure 4.6. The

design utilizes modulation doped InP spacer, which reduces the alignment constraints of the gate. The modulation doping keeps the access resistance low even for fairly long spacer regions. This led to that a device with 40 nm gate overlap has a comparable performance to a spacer less design with a precisely positioned gate (gate overlap of ~5 nm). The device exhibits a C_{gg} = 1.0 fF/µm, but due to relatively poor transconductance of both devices with and without spacer, the f_T and f_{max} was 70 and 100 GHz respectively.

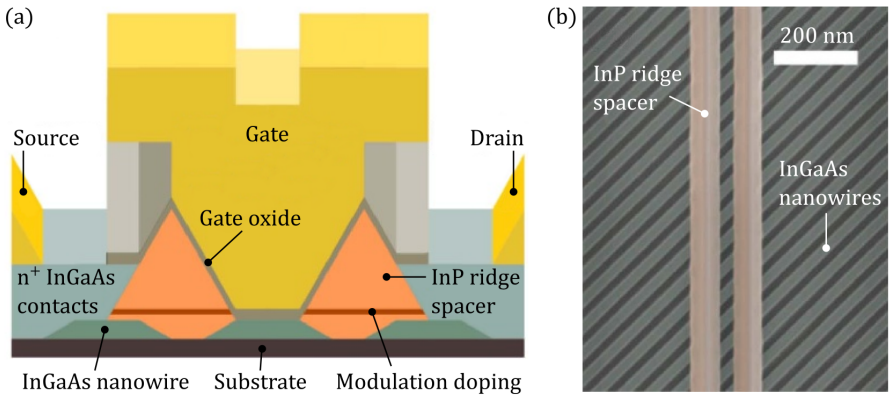

Figure 4.6: [68] (a) Schematic figure of the MOSFET structure. The InP ridges relax the gate alignment requirements, and the modulation doping is beneficial for reducing access resistance. (b) SEM image of a device after the growth of the InP ridges. The nanowires have a thickness of 7 nm and a width of 30 nm.

4.3 CRYOGENIC TEMPERATURE CHARACTERIZATION

The InGaAs nanowire platform was used to fabricate a network of nanowires. Gates were placed on the nanowires in such a way to be able to route the current through a specific path of the network. This is the basis of a multiplexing/demultiplexing circuit, which converts many inputs to fewer outputs. In paper VI a 1-to-4 demultiplexing circuit was fabricated and characterized at room temperature and cryogenic temperatures down to 40 mK. The device structure is shown in figure 4.7. The process has good yield with over 95 % of the current paths working, confirmed by measurements on 8 different multiplexers. The total median inverse subthreshold slope of all current paths is ~10 mV/dec at 13 K, indicating good electrostatic control.

Transfer characteristics for one current path obtained at 13 K and 40 mK can be seen in figure 4.8(a). Only one demultiplexer has been characterized

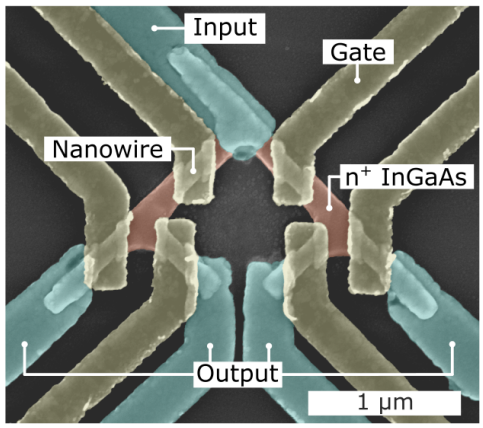

Figure 4.7: [69] False-colored SEM image of a nanowire network demultiplexer. The nanowire channels have dimensions of W = 80 nm and L_G = 120 nm. By turning on or off specific gates, the current can be routed from the input to one of the selected outputs.

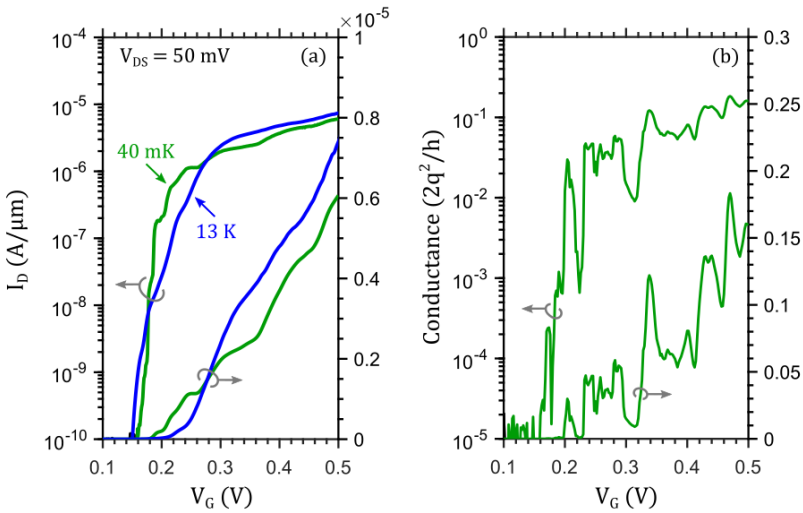

Figure 4.8: [69] (a) Transfer characteristics obtained at 13 K and 40 mK. The current is normalized to the nanowire width. (b) Normalized conductance measured with V_{DS} = 5 mV at 40 mK.

at 40 mK due to the necessity of bonding the device to a holder with limited number of bonding pads. A reduction in average inverse subthreshold slope is observed with reduction in temperature, with a $S_{min} = 2$ mV/dec at 40 mK. This steep slope is attributed to potential fluctuations in the conduction band edge leading to a 1D resonant tunneling type behavior. The potential fluctuations are believed to originate from charged defects at the semiconductor/oxide interface. Figure 4.8(b) shows the conductance of the same current path obtained at 40 mK and a low drain bias of 5 mV. At this small bias window, the conductance breaks up into several peaks due to the potential fluctuations in the conduction band edge along the channel. This gives rise to peaks in the transmission at certain energies, indicating the importance of a defect free semiconductor/oxide interface for good performance, especially for operation at cryogenic temperatures.

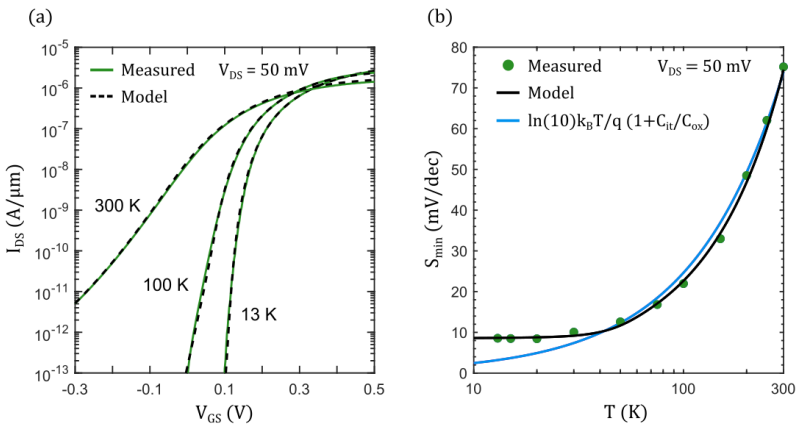

Figure 4.9: (a) Transfer characteristics at 13, 100 and 300 K with $V_{DS} = 50$ mV. Together with the fitted model. (b) Measured and simulated temperature dependence of the minimum inverse subthreshold slope.

In paper VII the temperature dependence of the current characteristics of a long channel InGaAs quantum well MOSFET was investigated. The fabricated device was characterized down to 13 K and showed a peak on-state mobility of 6700 cm^2/Vs and minimum inverse subthreshold slope of 8 mV/dec which is much larger than predicted by Boltzmann statistics. A model including band tail states, interface traps and a electron concentration dependent mobility was developed to accurately explain the measured data. Figure 4.9(a) shows the transfer characteristics obtained at 13, 100 and 300 K together with the fitted model. In figure 4.9(b) the minimum inverse subthreshold slope can be seen. The electron concentration dependent mobility can be understood as

followed. At low gate bias the conducting electrons are close to the conduction band edge, where the fluctuating potential due to disorders is reducing the mobility. Increasing the gate bias will increase the mobility due to increased screening which reduces the scattering. At some gate voltage the mobility will start to reduce again due to that the electron wave function is pushed closer to the semiconductor/oxide interface, which increases the interaction with interface defects.

5

Conclusion and Outlook

Work in this thesis has explored many different aspects of InGaAs nanowire and quantum well devices. The fabricated devices have been characterized by I-V, C-V and Hall measurements over a wide temperature range. At cryogenic temperatures the impact of band tails states on the inverse subthreshold slope has been investigated, as well as the gate voltage dependence of the mobility. A multiplexing/demultiplexing device structure has been implemented using a selective area grown InGaAs nanowire network. This concept device has been analyzed in detail at temperatures down to 40 mK. At low applied bias voltage conductance peaks are observed, which are attributed to potential fluctuations in the conduction band edge caused by defects in the semiconductor/oxide interface. Near surface quantum well devices have been investigated to understand the impact of surface defects on the electron transport. Moving the defect dense interface away from the conducting electrons can greatly improve the electron mobility.

For RF compatible MOSFETs, different spacer technology schemes have been developed and the intrinsic and extrinsic capacitances have been studied. The devices show low capacitances, which is important for viability in high-frequency applications. To further increase RF performance an increase of transconductance and decrease of output conductance is needed. This can be achieved by refining the quality of the channel and reducing the defect density in the semiconductor/oxide interface. The transparency of the contacts is also important for the extrinsic device performance.

For devices operating at low temperatures reducing disorder/defects impacting the transport is vital for device performance. Work of using atomic hydrogen annealing to clean the semiconductor surface in order to improve interfaces is ongoing. This can be useful both for decreasing disorder in the semiconductor/oxide interface or for more transparent contacts. There

is also ongoing work with using the nanowire process platform for creating semiconductor-superconductor proximitized devices for topological quantum computing.

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APPENDICES

A

Lateral Nanowire MOSFET Process

In this appendix, a detail description of the process steps are given. The (100) InP:Fe semi-insulating wafers are bought from InPACT. The growth has been done using a horizontal MOCVD system Aixtron 200/4 with the following precursors; TMGa, TMIn, TESn, AsH_3 and PH_3.

A.1 DC MOSFET FABRICATION

A.1.1 NANOWIRE FORMATION

- **Sample preparation**
  Cut (100) InP (S.I) wafer into 8 $\times$ 10 mm pieces

- **Organic cleaning**
  2 min in acetone, 1 min in ultra-sonic bath
  2 min in acetone, 2 min in iso-2-propanol (IPA)

- **Ozone cleaning**
  10 min ozone cleaning, 500 sccm O_2 flow
  $\rightarrow$ *A properly oxidized surface improves HSQ adhesion.*

- **Resist deposition**
  2 min on 200 °C hotplate.
  Spin coat 2% HSQ at 6000 rpm (3000 rpm/s) for 60 s
  Bake resist 2 min on 200 °C hotplate
  $\rightarrow$ *The HSQ thickness is roughly 30 nm. A high baking temperature improves*

the HSQ adhesion but contrast will be decreased.

- **EBL 1: Nanowire**
  Exposure of nanowire growth mask using acceleration voltage of 50 kV, 30 µm aperture and 2 nm step size.

- **Resist development and surface cleaning**
  90 s in TMAH (25%) heated to 40°C, 1 min in H_2O, 30 s in IPA
  60 min in RTP at 350 °C, 150 l/h O_2
  Just before growth, 20 s in HF (1:1000), 30 s in H_2O
  → *Elevated development temperature increases contrast but higher dose is also needed. The short HF dip removes surface oxides which is crucial for limiting defect density at the beginning of the growth. The diluted HF will also slightly etch the HSQ mask, the HSQ etch resistance is improved by the RTP step.*

- **Nanowire growth**
  Growth of 13 nm $In_{0.65}Ga_{0.35}As$ at 600 °C

- **HSQ removal and contrast enhancement**
  4 min in BOE (10:1), 1 min in H_2O
  4 s in HCl:H_2O (1:1), 1 min in H_2O, 30 s in IPA
  → *The InP etch rate is roughly 4 nm/s. The purpose of the InP etch at this stage is mainly to improve the depth of the EBL markers.*

A.1.2 DUMMY GATE AND CONTACT REGROWTH

- **Resist deposition**
  2 min on 200 °C hotplate.
  Spin coat 2% HSQ at 6000 rpm (3000 rpm/s) for 60 s
  Bake resist 2 min on 200 °C hotplate.

- **EBL 2: Dummy gate**
  Exposure of dummy gate features using acceleration voltage of 50 kV, 40 µm aperture and 8 nm step size.

- **Resist development**
  90 s in TMAH (25%) heated to 40°C, 1 min in H_2O, 30 s in IPA
  → *This could also be done at room temperature depending on the target gate lengths.*

- **Contact regrowth**
  Growth of 30 nm $In_{0.63}Ga_{0.37}As$ doped with Sn at 600 °C

- **HSQ removal**
  4 min in BOE (10:1), 1 min in H_2O, 30 s in IPA

A.1.3 MESA FORMATION

- **Resist deposition**
  2 min on 200 °C hotplate.
  Spin coat FOx15 at 6000 rpm (2000 rpm/s) for 60 s
  Bake resist 2 min on 200 °C hotplate

- **EBL 3: Mesa**
  Exposure of mesa etch mask using acceleration voltage of 50 kV, 40 µm aperture and 8 nm step size.

- **Resist development**
  90 s in TMAH (25%), 1 min in H_2O, 30 s in IPA
  Bake resist 5 min on 200 °C hotplate

- **Mesa wet etch**
  35s in H_3PO_4:H_2O_2:H_2O (1:1:25), 1 min in H_2O, 30 s IPA

- **SiN_x deposition**
  PECVD deposition of 14 nm SiN_x at 200 °C

- **HSQ removal**
  90 s in BOE (10:1), 1 min in H_2O, 30 s in IPA
  → *The SiN_x will also be etched by roughly 5 nm/min.*

- **Pillar etch and digital etch**
  8 min ozone cleaning, 500 sccm O_2 flow
  4 s in HCl:H_2O (1:1), 1 min in H_2O
  8 min ozone cleaning, 500 sccm O_2 flow
  15 s in HCl (1:10), 30 s in H_2O, 30 s in IPA
  → *Each digital etch cycle removes roughly 1.4 nm.*

A.1.4 CONTACT METALLIZATION

- **Resist deposition**
  2 min on 200 °C hotplate.
  Spin coat PMMA 950 A4 at 4500 rpm (1500 rpm/s) for 60 s
  Bake resist 2 min 15 s on 180 °C hotplate

- **EBL 4: Source and drain contacts**
  Exposure using acceleration voltage of 50 kV, 40 µm aperture and 8 nm step size.

- **Resist development**
  90 s in methyl isobutyl ketone (MIBK):IPA (1:3), 30 s in IPA

- **Metallization: Source and drain contacts**
  35 s in oxygen plasma etcher, 5 mbar O_2 pressure
  20 s in HCl:H_2O (1:20), 30 s in H_2O
  E-beam evaporation of Ti/Pd/Au (5/5/40 nm)

- **Lift-off**
  2 h in acetone, 30 s in IPA
  35 s in oxygen plasma etcher, 5 mbar O_2 pressure

A.1.5 SOURCE AND DRAIN PADS

The pads can either be defined by UVL or EBL depending on alignment requirements.

UVL Pads

- **Resist deposition**
  5 min on 110 °C hotplate.
  Spin coat ma-N 440 at 6000 rpm (1500 rpm/s) for 45 s
  Bake resist 3 min on 95 °C hotplate

- **UV exposure**
  Hard contact mode, 50 s exposure

- **Resist development**
  105 s in ma-D 532/S, 1 min H_2O

- **Metallization: Pads**
  35 s in oxygen plasma etcher, 5 mbar O_2 pressure
  E-beam evaporation of Ti/Pd/Au (5/5/200 nm)

- **Lift-off**
  2 h in acetone, 30 s in IPA
  35 s in oxygen plasma etcher, 5 mbar O_2 pressure

EBL Pads

- **Resist deposition**
  2 min on 200 °C hotplate.
  Spin coat PMMA 950 A8 at 4500 rpm (1500 rpm/s) for 60 s
  Bake resist 2 min 15 s on 180 °C hotplate

- **EBL: Pads**
  Exposure using acceleration voltage of 50 kV, 40 µm aperture and 8 nm step size.

- **Resist development**
  90 s in methyl isobutyl ketone (MIBK):IPA (1:3), 30 s in IPA

- **Metallization: Source and drain contacts**
  35 s in oxygen plasma etcher, 5 mbar O_2 pressure
  E-beam evaporation of Ti/Pd/Au (5/5/200 nm)

- **Lift-off**
  2 h in acetone, 30 s in IPA
  35 s in oxygen plasma etcher, 5 mbar O_2 pressure

A.1.6 GATE OXIDE DEPOSITION

- **Surface cleaning and passivation**
  2 min in acetone, 1 min in IPA
  8 min ozone cleaning, 500 sccm O_2 flow
  20 min in $(NH_4)_2S_x$ (10 % in H_2O), 7 s in H_2O
  Directly put in ALD chamber

- **Oxide deposition**
  5 cycles of TMAl
  7 cycles of Al_2O_3 at 300 °C

100 cycles of HfO_2 at 120 °C

A.1.7 GATE METALLIZATION

- **Resist deposition**
  2 min on 200 °C hotplate.
  Spin coat PMMA 950 A4 at 4500 rpm (1500 rpm/s) for 60 s
  Bake resist 2 min 15 s on 180 °C hotplate

- **EBL 5: Gate**
  Exposure using acceleration voltage of 50 kV, 40 µm aperture and 8 nm step size.

- **Resist development**
  90 s in MIBK:IPA (1:3), 30 s in IPA

- **Metallization: Gate**
  35 s in oxygen plasma etcher, 5 mbar O_2 pressure
  E-beam evaporation of Ti/Pd/Au (5/5/40 nm)

- **Lift-off**
  2 h in acetone, 30 s in IPA
  35 s in oxygen plasma etcher, 5 mbar O_2 pressure

A.1.8 GATE PAD

Same recipe as the source and drain pads.