LUND UNIVERSITY

As-deposited ferroelectric HZO on a III–V semiconductor

Andersen, André; Persson, Anton E. O.; Wernersson, Lars-erik

Published in:
Applied Physics Letters

DOI:
10.1063/5.0097462

2022

Document Version:
Peer reviewed version (aka post-print)

Link to publication

Citation for published version (APA):
Andersen, A., Persson, A. E. O., & Wernersson, L. (2022). As-deposited ferroelectric HZO on a III–V semiconductor. *Applied Physics Letters*, *121*(1), 012901. https://doi.org/10.1063/5.0097462

Total number of authors:
3

Creative Commons License:
CC BY

General rights
Unless other specific re-use rights are stated the following general rights apply:
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.
• Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
• You may not further distribute the material or use it for any profit-making activity or commercial gain
• You may freely distribute the URL identifying the publication in the public portal

Read more about Creative commons licenses: https://creativecommons.org/licenses/

Take down policy
If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

LUND UNIVERSITY

PO Box 117
221 00 Lund
+46 46-222 00 00

As-deposited ferroelectric HZO on a III-V semiconductor

André Andersen,[1, a)] Anton E. O. Persson,[1] and Lars-Erik Wernersson[1, b)]

Affiliations

[1]*Electrical and Information Technology, Lund University, Lund, Box 118, 22100, Sweden*

Authors to whom correspondence should be addressed:
[André Andersen, andre.andersen@eit.lth.se; Lars-Erik Wernersson, lars-erik.wernersson@eit.lth.se]

Abstract

By electrical characterization of thin films deposited by atomic layer deposition (ALD), $Hf_xZr_{1-x}O_2$ (HZO) is shown to be ferroelectric as-deposited, i.e., without any annealing step, using a thermal budget of 300 °C. By fabricating laminated HZO films rather than the traditional solid-solution HZO, a remanent polarization of P_r = 11 µC/cm^2 and endurance exceeding 10^6 are obtained. Films grown on thermally reactive InAs semiconductor substrates showed capacitance-voltage modulation and hysteresis, which varied depending on interfacial oxide construction. Additionally, a trade-off between higher polarization and lower gate leakage was found when comparing different laminate structures and deposition temperatures. Scaling the thickness of the laminated oxides revealed that films remain ferroelectric at 6.5 nm, with an increased breakdown field for thinner devices.

Since the discovery of ferroelectric HfO_2,[1] there has been ever-increasing efforts to integrate the material in emerging device concepts.[2–5] New technology includes memory devices able to surmount the von-Neumann barrier,[2] and negative capacitance transistors that enable steep-slope switching.[3] For high performance devices, it is also important to demonstrate ferroelectric compatibility with III-V compound semiconductors, which offer transport properties superior to Si.[6] But a major roadblock in the implementation of ferroelectric oxides on III-V semiconductors is the high processing temperatures associated with achieving the non-centrosymmetric, orthorhombic phase (o-phase), that facilitates the ferroelectricity.[7]

Fabrication of ferroelectric HfO_2 usually starts with atomic layer deposition (ALD) of mainly amorphous oxide.[1] Following this step, a top metal capping layer is sputtered that imparts a biaxial tensile strain in the film below.[1,8,9] When the oxide is subsequently subjected to high-temperature, rapid thermal processing (RTP), the imposed strain will force the HfO_2 to settle into the ferroelectric orthorhombic crystal phase by suppressing the otherwise more stable monoclinic phase. The principal problem arises during RTP, where temperatures required can reach 1000 °C.[1] Several strategies have already been implemented to improve the thermal budget of HfO_2-based processes, and the most prominent of these are the introduction of dopants and other oxides.[10–12] The most popular method is adding alternating layers of ZrO_2, creating solid-solution HZO. The low crystallization temperature of ZrO_2 reduces the RTP temperatures for HZO to achieve o-phase crystallization.[13] Recently it has been demonstrated that the stacking sequence of the oxides can be modified to design laminates that drastically change the properties of the entire film.[14–17]

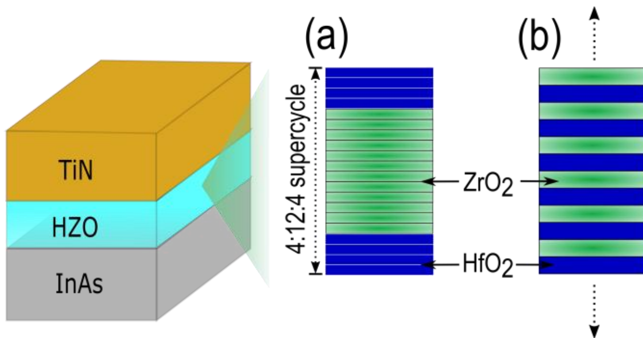


Fig. 1. Schematic MOS structure with (a) a HZO laminate in 4:12:4 (Hf:Zr:Hf) configuration. Several supercycles are repeated to form the total oxide and (b) 1:1 solid-solution HZO.

In this study we focus on a type of laminate construction based on recent discoveries by Cheema et al..[15] Laminated HZO was implemented in metal-oxide-semiconductor capacitors (MOSCAPs) with InAs substrates to determine their viability on a temperature sensitive platform. Previous work by Persson et al. also found that solid-solution HZO grown on InAs offered reduced RTP temperatures with superior performance compared to metal-insulator-metal (MIM) stacks with equivalent oxide.[18] The laminated HZO investigated in this project was characterized as-deposited, meaning no RTP has been performed following top-metal capping (unless stated), and the highest processing temperature was during ALD of the oxide.

HZO laminates were integrated in MOSCAP structures, where the semiconductor consisted of epitaxial, non-intentionally n-doped (5×10^{17} cm^{-3}), 300-nm-thick InAs(111) layers grown on Si substrates using metal-organic vapor phase epitaxy. The samples were subjected to a HCl:H_2O wet etch (1:10) to remove the native oxide before being placed in a PicoSun R100 ALD chamber. The precursors used for HfO_2 and ZrO_2 deposition were Tetrakis(dimethylamido)hafnium (TDMAHf) and Tetrakis(ethylmethylamido)zirconium (TEMAZr), respectively, while H_2O was used as oxidizer. The growth temperature was either 300 or 325 °C, and the ALD stacking sequence was varied to grow laminates of three different structures presented as a ratio x:y:x, corresponding to the number of internal ALD cycles in the form HfO_2:ZrO_2:HfO_2, starting with HfO_2 towards the substrate. The laminate was then repeated for several supercycles to reach a targeted thickness (e.g., seven supercycles of 4:12:4 laminates result in a ~14 nm oxide, assuming a growth rate per cycle (GPC) of 1 Å/cycle). In Fig. 1(a) the construction of a single supercycle 4:12:4 laminate is shown. Following ALD, a 10 nm TiN capping layer was sputtered, and the process was finalized by a lift-off/evaporation step to define Ti/Au contacts (5/200 nm) used as masks for TiN etching and for probing. The laminate structures investigated were 4:12:4, 5:15:5, and 6:18:6, all consisting of nominally 60 at% ZrO_2 deposited for four to seven supercycles. A solid-solution HZO sample with the oxide deposited at 300 °C was added as a reference (see Fig. 1(b)). Two additional MOSCAPs with 4:12:4, 7 supercycle laminate were produced with different interfaces and compared to the HfO_2 interface of the 4:12:4, 7 supercycle sample deposited at 300 °C. One sample had the first 4 cycles of HfO_2 removed when forming the oxide, with 12 cycles of ZrO_2 towards the substrate. The other sample had the same laminate structure as Fig. 1(a), except it had 6 ALD cycles of Al_2O_3 grown at the interface. This was done to study the effect of the interfacial layers on the gate capacitance and defect response close to the interface, which is critical for future ferroelectric field-effect transistor (FeFET) performance.[19] The Al_2O_3 interface is desirable since it has been shown to reduce the amount of native As-oxide at the InAs interface, which is desirable for high performance FET devices.[20] The aluminum oxide was deposited at 300 °C using trimethylaluminium (TMA). The procedures described above, excluding the HCl wet etch, were also performed on a sputtered TiN (10nm)/Si substrate for a reference metal-insulator-metal capacitor (MIMCAP). It was prepared with a 4:12:4 laminated, 7 supercycle oxide, deposited at 300 °C.

The thickness of the oxides was evaluated using a Woollam RC2 ellipsometer (the GPC of each laminate structure can be found in the supplementary material, Fig. S1). The electrical characterization was primarily performed using a MPITS200-SE semi-automatic probe station with a Keysight B1500A parameter analyzer, equipped with a B1530 waveform generator for pulsed measurements. The measurements performed were DC IV-sweeps to determine gate leakage, and the positive-up, negative-down (PUND) technique to evaluate polarization-electric field (P-E) curves of the ferroelectrics.[21] Moreover, room temperature and cryogenic (~30 K) CV-measurements were performed using a CRX-4K cryogenic probe station and an Agilent 4294A impedance analyzer. During the CV measurements, the small-signal frequency was varied, while the amplitude was kept at 50 mV. In addition to electrical measurements, Grazing Incidence X-ray Diffraction (GIXRD) was also performed using a Bruker D8 Discover equipped with a Cu K-α source.

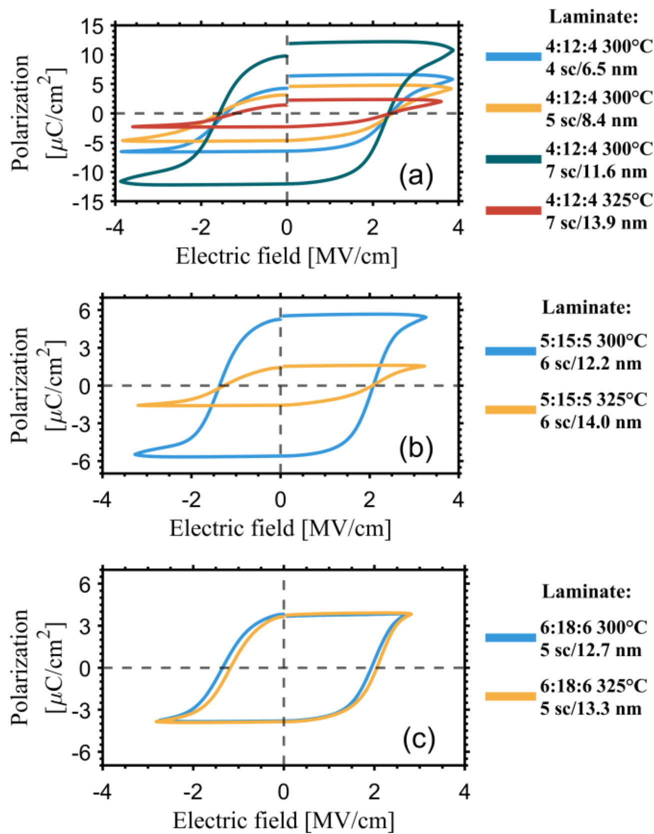


Fig. 2. Polarization-Electric field (P-E) characteristics of different HZO laminates, deposited at 300 °C and 325 °C. PUND measurements were performed at 1 kHz, following 2000 rectangular wake-up cycles with the same amplitude as the corresponding PUND pulse. P-E curves are evaluated for (a) 4:12:4 laminates grown for different numbers of supercycles (4, 5, and 7), resulting in different thicknesses (b) 5:15:5 laminates grown for 76 supercycles and (c) 6:18:6 laminates grown for 75 supercycles.

PUND measurements performed on as-deposited films (Fig. 2) revealed ferroelectric polarization switching in all as-deposited samples (compare this to the solid-solution HZO reference, which only showed very weak polarization, found in the supplementary material, Fig. S2). The ferroelectricity of a laminate structured oxide was also confirmed using XRD, available in supplementary material Fig. S3. Fig. 2(a) contains the P-E curves for a 4:12:4 laminated structure grown for different numbers of supercycles (four, five, and seven supercycles, respectively) and temperatures, resulting in different thicknesses. The result shows that ferroelectric polarization remains even when the oxide is scaled down to 6.5 nm thickness. The high (positive) coercive fields (E^{+}_{c}~2.4 MV/cm) that are required for polarization switching give rise to leakage, distorting the top of some P-E curves (see Fig. 2(a)). To gauge the practical ferroelectricity of the samples, P-E curves measured using bipolar triangular pulses, rather than PUND, are provided in supplementary material Fig. S4. The coercive field is higher compared to previous values for solid-solution HZO on InAs (which had been subjected to high temperature RTP), where the E_c typically ranges from 1-2 MV/cm.[18] This is also the range for reported other methods that achieve low-temperature ferroelectric HZO.[22–25] The asymmetrical coercive field, most clearly seen in Fig. 2(a) and 2(c), results from the difference in work function for TiN and InAs, and internal bias fields that can arise from defect charge traps interfaces.[26] Comparing the results presented in Fig. 2(a-c), the general trend shows a more consistent ferroelectric phase formation for deposition at 300 °C as compared to 325 °C. This could be related to a higher degree of TEMAZr-degradation at 325 °C, since the ALD-precursor have previously shown thermal instability in this temperature range.[27] Notably, for the 6:18:6 laminates the 325 °C deposition temperature facilitated similar remanent polarization compared to deposition at 300 °C, which opposed the trend observed in the other two laminate structures. These samples have thicker ZrO_2 stacks in the laminates, that could broaden the ALD process window enough to facilitate more ferroelectric crystallization.

The ferroelectricity in the laminates is believed to be caused by increased strain in both the ZrO_2 and HfO_2 stack, compared to solid-solution HZO.[15] The highest as-deposited remanent polarization on InAs was found in the 7 supercycle 4:12:4 laminate and could be approximated to $P_r \approx 11$ μC/cm^2 from Fig. 2(a), when omitting the distortion caused by leakage. The 4:12:4, 4 supercycle laminate had a lower remanent polarization of $P_r = 5$ μC/cm^2 but remained ferroelectric when scaled. This is important for device application as solid-solution HZO requires increased RTP temperature when scaled to remain ferroelectric.[28] The literature related to as-deposited ferroelectricity is sparse but there is a similar result using strain-inducing TiO_2 interlayers to form

laminates, achieving a P_r value of 3.7 μC/cm^2 with a thermal budget of 300 °C.[22] It is worth noting that films fabricated using different BEOL compatible methods have shown both similar, and higher P_r values (exceeding 20 μC/cm^2) when grown on metal substrates, with the same thermal budget.[23–25] The MIMCAP reference showed a remanent polarization of P_r = 12 μC/cm^2, at significantly lower fields (E_c^+~1.3 MV/cm, available in supplementary material, Fig. S5), suggesting as-deposited films on metal substrates tend to reach higher o-phase fraction, regardless of oxide design. Although the film properties on metal bottom-electrodes can provide useful insights for design of ferroelectric tunnel junctions,[2] the behavior on semiconductor substrates is critical for integration on transistor platforms. Several studies instead focus on reducing the annealing temperatures, rather than realizing ferroelectricity in as-deposited films.[18,29] In our study, a similar approach was also taken for several of the 7 supercycle laminates, but no clear improvement in the remanent polarization was achieved until RTP at 450 °C for 300 s, after which a remanent polarization of P_r = 14 μC/cm^2 was measured (available in supplementary material, Fig. S6).

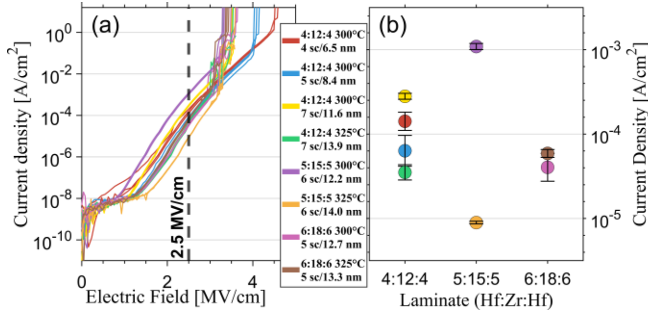


Fig. 3. The leakage of various laminated oxides quantified by the (a) J-E curve showing the behavior for an electric field sweep and (b) the leakage calculated according to the dashed line at 2.5 MV/cm.

In Fig. 3(a) the current density of various laminated HZO is plotted as a function of the electric field while Fig. 3(b) shows the leakage current density measured at an electric field of 2.5 MV/cm. Most notably, the four and five supercycle oxides (6.5 and 8.4 nm, respectively) outperforms the thicker samples in breakdown voltage (4.5 and 4 MV/cm respectively, compared to ~3.5 MV/cm for the thicker samples), confirming the promising scaling trend seen previously for solid-solution HZO.[28] The 4:12:4 and 5:15:5 laminates deposited at 300 °C showed more leakage than the laminates deposited at 325 °C, but also had higher remanent polarization. The leakage of these samples at 2.5 MV/cm also agrees with what has previously been reported for low thermal budget HZO.[24] This could be related to the formation of grain boundaries along o-phase domains which are not as prevalent in less crystalline films.[30] Note that the 6:18:6 laminated oxides both have similar polarization and leakage despite the different deposition temperatures.

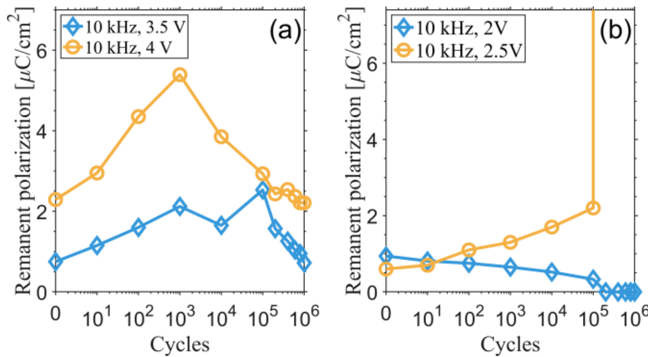


Fig. 4. The ferroelectric endurance of 4:12:4 laminate oxides at two different thicknesses. (a) The endurance of a 7 supercycle laminate (11.6 nm) with 10 kHz triangular pulses performed at two different voltage amplitudes, corresponding to fields above the coercive field in both bias directions. (b) The endurance of the 4 supercycle (6.5 nm) oxide, also with 10 kHz triangular pulses performed at different voltage amplitudes. The vertical line is the point of oxide breakdown.

In Fig. 4(a), the endurance of the 4:12:4 laminates deposited at 300 °C is presented (the laminates with highest P_r on InAs). The endurance test is performed at lower electric fields, higher pulse frequency, and with triangular pulses (as opposed to rectangular wake-up pulses). This results in lower remanent polarization compared to Fig. 2, but it mimics more realistic device application. For the seven supercycle oxide, the remanent polarization is significantly higher after the film is stressed with larger voltage amplitudes. The higher field allows a higher fraction of the ferroelectric domains to switch. For both voltage amplitudes the wake-up effect[31] can clearly be seen. After 10^5 (3.5 V pulses) and 10^3 (4 V pulses) the performance of the films starts to degrade

significantly. This decrease has previously been observed in other reports,[32,33] and it is believed to be related to the redistribution of defects in both the bulk and interface of the oxide.[34] This eventually also leads to oxide breakdown as vacancies are generated that act as new leakage paths.[34] Although the films endure 10^6 cycles, the wake-up and fatigue effect is undesirable since it can cause device variation over time. The effect is very pronounced in the laminates adopted here compared to another low thermal budget method (atomic layer annealing), which offers flat remanent polarization up to at least 10^4 cycles.[25] Similar measurements were also performed on the 4 supercycle, 4:12:4 laminate at different voltages (see Fig 4(b)). The 2.5 V pulses resulted in wake-up followed by earlier breakdown, rather than decreased polarization. The 2 V pulses did not facilitate any wake-up effect, but the endurance was significantly improved.

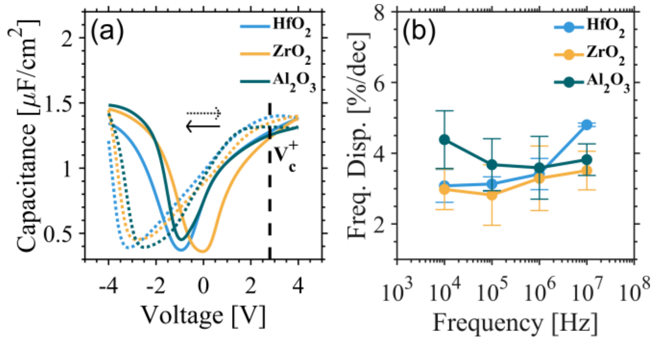


Fig. 5 Capacitance-Voltage sweeps of 4:12:4 laminate (7 supercycles) MOSCAPs with different interfaces (HfO_2, ZrO_2 and Al_2O_3) towards the InAs substrate. (a) Capacitance-voltage characteristics of the different interface samples. The measurement was performed at 30 K with a small signal frequency of 1 MHz. The dashed black line corresponds to the positive coercive voltage of the HfO_2 interface sample. (b) The frequency dispersion for the same samples. The dispersion was collected in accumulation (3 V) at a temperature of 30 K.

The measured CV characteristic and its hysteresis of 4:12:4 laminates with different interfaces, grown at 300 °C, is presented in Fig. 5 (a), where the arrows show the sweep direction. CV measurements were performed at cryogenic temperatures (30K) to avoid leakage currents and oxide breakdown during the DC bias sweep. The weak capacitance-peak in accumulation of the HfO_2-interface film centered at approximately 2.8 V agrees with the coercive field of the film and represents the expected CV behavior in ferroelectric films.[11] A clearer example of this can be found in the supplementary materials (Fig. S7) together with CV data for the as-deposited MIM reference (Fig. S8), that shows the more traditional ferroelectric "butterfly"-characteristic. Previous studies on InAs based MOSCAPs revealed a clear suppression of minority carries and border traps at high frequency and cryogenic CV characterization, depleting the minority carrier in the semiconductor.[18,19,35] This was attributed to the slow response time of minority carrier and border trap charges at low temperatures. Notably, in Fig. 5(a) there is a strong response at negative voltages for all samples, which is attributed to the substrate used this study (epitaxial InAs on Si rather than InAs substrates) with a higher minority generation rate, combined with a potentially increased defect density in the vicinity of the oxide-semiconductor interface. Despite this, the steep capacitance-modulation in the left-to-right sweep suggests low interface trap-densities.[36] The large hysteresis is believed to originate from charging of border traps, an effect that has previously been shown to be exacerbated in ZrO_2 rich films when sweeping to and from high accumulation voltages.[35] The presence of border traps, in conjunction with fixed oxide charges could cause a large shift in the threshold voltage.[37]

Finally, the spatial distribution of border traps close to the interfaces was investigated using frequency dispersion in accumulation at 3 V (see Fig. 5(b)) at 30 K.[19] The data revealed that the HZO/HfO_2/InAs and HZO/ZrO_2/InAs interface had similar and lower relative concentration of interface traps compared to HZO/Al_2O_3/InAs for frequencies up to 1 MHz, which agrees with previous studies of ferroelectric HZO on InAs with, and without, an Al_2O_3 interface layer.[9,19] At even higher frequencies the HZO/HfO_2/InAs interface showed somewhat higher dispersion, which suggests that it has a slightly higher concentration of traps closest to the interface. This, however, does not seem to have affected the crystallization as it showed the highest degree of ferroelectric polarization of the three samples (11 $\mu C/cm^2$). The other samples had $P_r = 2.2$ and 3.5 $\mu C/cm^2$ for the ZrO_2/InAs and Al_2O_3/InAs interface, respectively (see supplementary material, Fig. S9). The higher polarization present in the Al_2O_3 interface sample compared to the ZrO_2 interface sample could be attributed to its ability to reduce InAs interfacial oxides.[20]

In conclusion, we have investigated the electrical properties of as-deposited, ferroelectric HZO on InAs. Different laminate structures were grown at 300 °C and 325 °C using ALD, and the data was compared to find that the optimal oxide construction which maximized the remanent polarization was 4:12:4 (HfO_2:ZrO_2:HfO_2) deposited at 300 °C. This laminate was repeated for several "supercycles" to fabricate oxides of different thicknesses, and it was found that the thinnest samples investigated (6.5 nm) remained ferroelectric, which is promising for future device integration. The 4:12:4 laminated oxide

with the highest polarization (and thickness of 11.6 nm) showed endurance up to 10^6 cycles. It was revealed that changing the interfacial layer towards the substrate could modify the CV and dispersion-characteristics of the MOS devices, but directly integrating HfO_2 towards InAs offered the highest polarization.

The supplementary material has additional electrical characterization that supports and complements the findings of this paper.

Acknowledgements

This work was supported in part by the European Research Council (grant id: 101019147) and in part by the Swedish Research Council (VR).

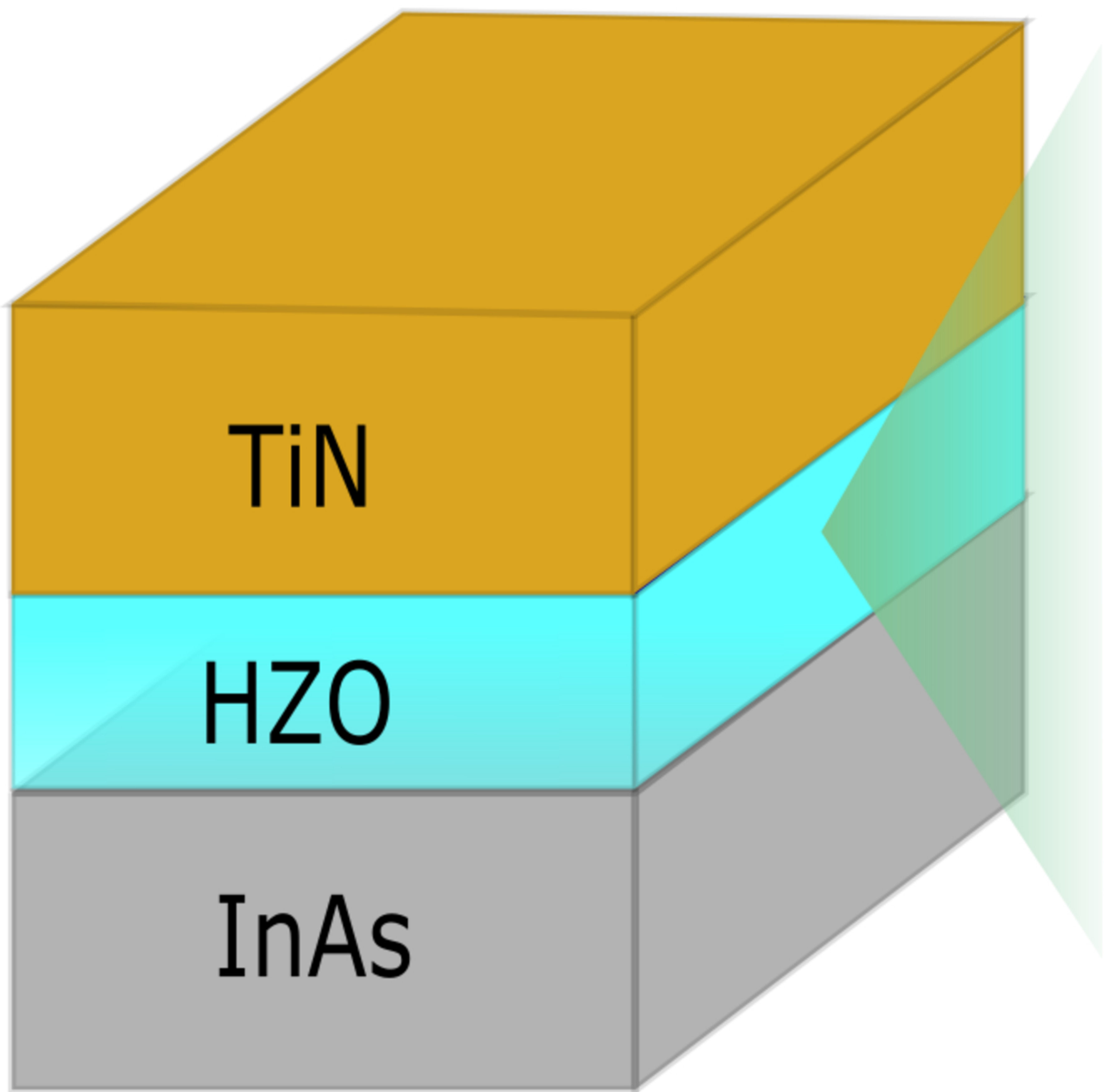
Data availability

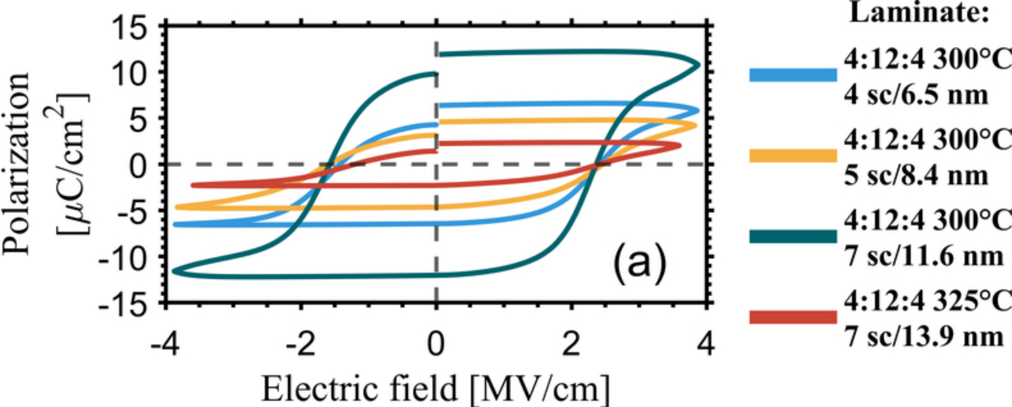
Any of the supporting data will be provided by the corresponding authors upon reasonable request.

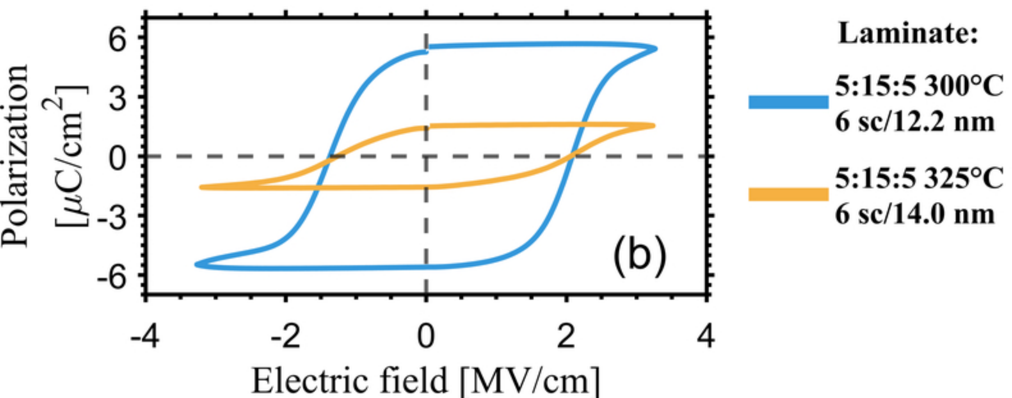
References

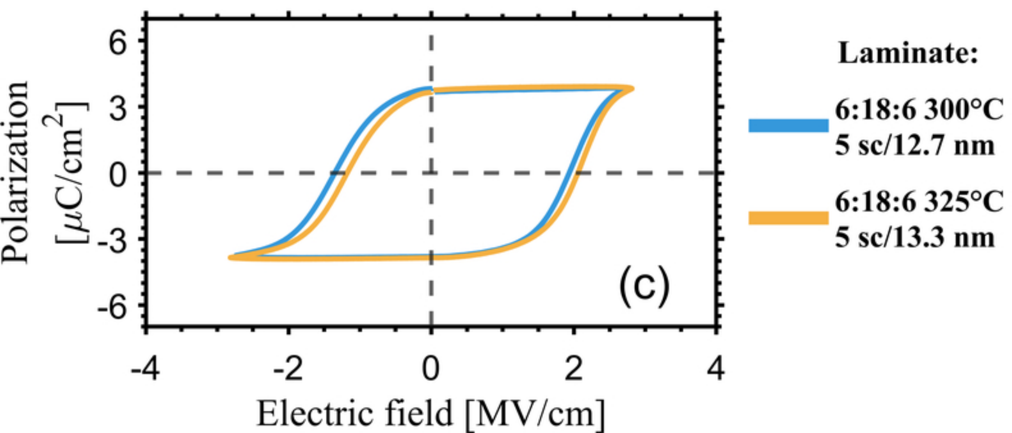
[1] T.S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger, Applied Physics Letters **99**, 102903 (2011).
[2] T. Mikolajick, U. Schroeder, and S. Slesazeck, IEEE Transactions on Electron Devices **67**, 1434 (2020).
[3] M. Hoffmann, S. Slesazeck, and T. Mikolajick, APL Materials **9**, (2021).
[4] S. Dunkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M. Majer, S. Wittek, B. Muller, T. Melde, H. Mulaosmanovic, S. Slesazeck, S. Muller, J. Ocker, M. Noack, D.-A. Lohr, P. Polakowski, J. Muller, T. Mikolajick, J. Hontschel, B. Rice, J. Pellerin, and S. Beyer, in *2017 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2017), pp. 19.7.1-19.7.4.
[5] H. Ryu, H. Wu, F. Rao, and W. Zhu, Scientific Reports **9**, (2019).
[6] H. Riel, L.E. Wernersson, M. Hong, and J.A. del Alamo, MRS Bulletin **39**, 668 (2014).
[7] N. Kobayashi and Y. Kobayashi, Japanese Journal of Applied Physics **30**, L1699 (1991).
[8] H. Ryu, K. Xu, J. Kim, S. Kang, J. Guo, and W. Zhu, IEEE Transactions on Electron Devices **66**, 2359 (2019).
[9] R. Athle, A.E.O. Persson, A. Irish, H. Menon, R. Timm, and M. Borg, ACS Applied Materials & Interfaces **13**, 11089 (2021).
[10] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, and T. Mikolajick, Advanced Functional Materials **22**, 2412 (2012).
[11] J. Müller, T.S. Böscke, U. Schröder, S. Mueller, D. Bräuhaus, U. Böttger, L. Frey, and T. Mikolajick, Nano Letters **12**, 4318 (2012).
[12] J. Muller, T.S. Boscke, S. Muller, E. Yurchuk, P. Polakowski, J. Paul, D. Martin, T. Schenk, K. Khullar, A. Kersch, W. Weinreich, S. Riedel, K. Seidel, A. Kumar, T.M. Arruda, S. v. Kalinin, T. Schlosser, R. Boschke, R. van Bentum, U. Schroder, and T. Mikolajick, in *Technical Digest - International Electron Devices Meeting, IEDM* (2013).
[13] S.J. Kim, J. Mohan, S.R. Summerfelt, and J. Kim, JOM **71**, 246 (2019).
[14] Y. Peng, W. Xiao, Y. Liu, C. Jin, X. Deng, Y. Zhang, F. Liu, Y. Zheng, Y. Cheng, B. Chen, X. Yu, Y. Hao, and G. Han, IEEE Electron Device Letters **43**, 216 (2022).
[15] S.S. Cheema, N. Shanker, L.-C. Wang, C.-H. Hsu, S.-L. Hsu, Y.-H. Liao, M. San Jose, J. Gomez, W. Chakraborty, W. Li, J.-H. Bae, S.K. Volkman, D. Kwon, Y. Rho, G. Pinelli, R. Rastogi, D. Pipitone, C. Stull, M. Cook, B. Tyrrell, V.A. Stoica, Z. Zhang, J.W. Freeland, C.J. Tassone, A. Mehta, G. Saheli, D. Thompson, D.I. Suh, W.-T. Koo, K.-J. Nam, D.J. Jung, W.-B. Song, C.-H. Lin, S. Nam, J. Heo, N. Parihar, C.P. Grigoropoulos, P. Shafer, P. Fay, R. Ramesh, S. Mahapatra, J. Ciston, S. Datta, M. Mohamed, C. Hu, and S. Salahuddin, Nature **604**, 65 (2022).

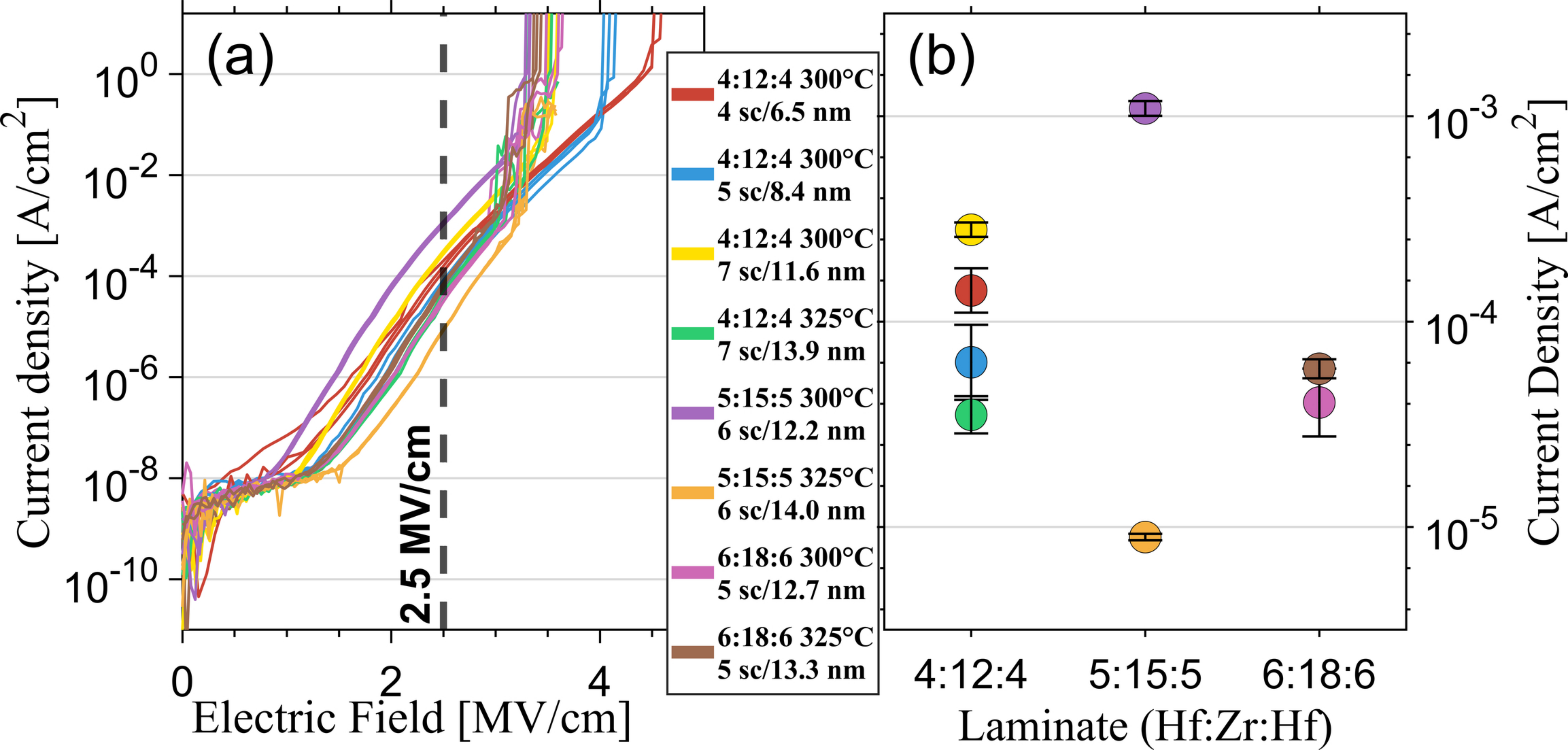
[16] T. Ali, K. Kühnel, R. Olivo, D. Lehninger, F. Müller, M. Lederer, M. Rudolph, S. Oehler, K. Mertens, R. Hoffmann, K. Zimmermann, P. Schramm, J. Metzger, R. Binder, M. Czernohorsky, T. Kämpfe, K. Seidel, J. Müller, J. van Houdt, and L.M. Eng, Electronic Materials **2**, 344 (2021).
[17] A. Kashir, M. Ghiasabadi Farahani, S. Kamba, M. Yadav, and H. Hwang, ACS Applied Electronic Materials **3**, 5632 (2021).
[18] A.E.O. Persson, R. Athle, P. Littow, K.M. Persson, J. Svensson, M. Borg, and L.E. Wernersson, Applied Physics Letters **116**, (2020).
[19] A.E.O. Persson, R. Athle, J. Svensson, M. Borg, and L.-E. Wernersson, Applied Physics Letters **117**, 242902 (2020).
[20] R. Timm, A. Fian, M. Hjort, C. Thelander, E. Lind, J.N. Andersen, L.-E. Wernersson, and A. Mikkelsen, Applied Physics Letters **97**, 132904 (2010).
[21] M. Fukunaga and Y. Noda, Journal of the Physical Society of Japan **77**, 064706 (2008).
[22] Y. Qi, X. Xu, I. Krylov, and M. Eizenberg, Applied Physics Letters **118**, (2021).
[23] S.J. Kim, Y.C. Jung, J. Mohan, H.J. Kim, S.M. Rho, M.S. Kim, J.G. Yoo, H.R. Park, H. Hernandez-Arriaga, J.-H. Kim, H.T. Kim, D.H. Choi, J. Jung, S.M. Hwang, H. Sejoon Kim, H.J. Kim, and J. Kim, Applied Physics Letters **119**, 242901 (2021).
[24] T. Onaya, T. Nabatame, N. Sawamoto, A. Ohi, N. Ikeda, T. Nagata, and A. Ogura, Microelectronic Engineering **215**, 111013 (2019).
[25] T.-J. Chang, Y.-S. Jiang, S.-H. Yi, C.-Y. Chou, C.-I. Wang, H.-C. Lin, and M.-J. Chen, Applied Surface Science **591**, 153110 (2022).
[26] C. Richter, T. Schenk, M.H. Park, F.A. Tscharntke, E.D. Grimley, J.M. LeBeau, C. Zhou, C.M. Fancher, J.L. Jones, T. Mikolajick, and U. Schroeder, Advanced Electronic Materials **3**, (2017).
[27] J.S. Becker, E. Kim, and R.G. Gordon, Chemistry of Materials **16**, 3497 (2004).
[28] K. Tahara, K. Toprasertpong, Y. Hikosaka, K. Nakamura, H. Saito, M. Takenaka, and S. Takagi, 2021 Symposium on VLSI Technology **1**, 978 (2021).
[29] D.Q. Xiao, B. bin Luo, W. Xiong, X. Wu, D.W. Zhang, and S.J. Ding, IEEE Transactions on Electron Devices **68**, 6359 (2021).
[30] M.H. Lee, Y.T. Wei, K.Y. Chu, J.J. Huang, C.W. Chen, C.C. Cheng, M.J. Chen, H.Y. Lee, Y.S. Chen, L.H. Lee, and M.J. Tsai, IEEE Electron Device Letters **36**, 294 (2015).
[31] H.J. Kim, M.H. Park, Y.J. Kim, Y.H. Lee, T. Moon, K. do Kim, S.D. Hyun, and C.S. Hwang, Nanoscale **8**, 1383 (2016).
[32] J. Lyu, T. Song, I. Fina, and F. Sánchez, Nanoscale **12**, 11280 (2020).
[33] R. Cao, Q. Liu, M. Liu, B. Song, D. Shang, Y. Yang, Q. Luo, S. Wu, Y. Li, Y. Wang, and H. Lv, IEEE Electron Device Letters **40**, 1744 (2019).
[34] M. Pešić, F.P.G. Fengler, L. Larcher, A. Padovani, T. Schenk, E.D. Grimley, X. Sang, J.M. LeBeau, S. Slesazeck, U. Schroeder, and T. Mikolajick, Advanced Functional Materials **26**, 4601 (2016).
[35] A.S. Babadi, E. Lind, and L.-E. Wernersson, Applied Physics Letters **108**, 132904 (2016).
[36] D.A. Deen and J.G. Champlain, Applied Physics Letters **99**, 053501 (2011).
[37] J. Lin, S. Monaghan, K. Cherkaoui, I. Povey, É. O'Connor, B. Sheehan, and P. Hurley, Microelectronic Engineering **147**, 273 (2015).


TiN
HZO
InAs
(a)
4:12:4 supercycle
(b)
ZrO_2
HfO_2


Laminate:
4:12:4 300°C
4 sc/6.5 nm
4:12:4 300°C
5 sc/8.4 nm
4:12:4 300°C
7 sc/11.6 nm
4:12:4 325°C
7 sc/13.9 nm
(a)
Polarization [μC/cm2]
Electric field [MV/cm]


Laminate:
5:15:5 300°C
6 sc/12.2 nm
5:15:5 325°C
6 sc/14.0 nm
(b)
Polarization [μC/cm2]
Electric field [MV/cm]


Laminate:
6:18:6 300°C
5 sc/12.7 nm
6:18:6 325°C
5 sc/13.3 nm
(c)
Polarization [μC/cm2]
Electric field [MV/cm]


(a)
Current density [A/cm^2]
10^0
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
2.5 MV/cm
0
2
4
Electric Field [MV/cm]
4:12:4 300°C 4 sc/6.5 nm
4:12:4 300°C 5 sc/8.4 nm
4:12:4 300°C 7 sc/11.6 nm
4:12:4 325°C 7 sc/13.9 nm
5:15:5 300°C 6 sc/12.2 nm
5:15:5 325°C 6 sc/14.0 nm
6:18:6 300°C 5 sc/12.7 nm
6:18:6 325°C 5 sc/13.3 nm
(b)
10^{-3}
10^{-4}
10^{-5}
Current Density [A/cm^2]
4:12:4
5:15:5
6:18:6
Laminate (Hf:Zr:Hf)

(a)

10 kHz, 3.5 V
10 kHz, 4 V

Remanent polarization [$\mu C/cm^2$]

0
2
4
6

0
10^1
10^2
10^3
10^4
10^5
10^6

Cycles

(b)

10 kHz, 2V
10 kHz, 2.5V

Remanent polarization [$\mu C/cm^2$]

0
2
4
6

0
10^1
10^2
10^3
10^4
10^5
10^6

Cycles

(a)

Capacitance [μF/cm^2]

2

1.5

1

0.5

-4 -2 0 2 4

Voltage [V]

HfO_2

ZrO_2

Al_2O_3

V_c^+

(b)

Freq. Disp. [%/dec]

8

6

4

2

10^3 10^4 10^5 10^6 10^7 10^8

Frequency [Hz]

HfO_2

ZrO_2

Al_2O_3