Development of new characterization techniques for III-V nanowire devices

Persson, Olof

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Development of New Characterization Techniques for III-V Nanowire Devices

Olof Persson

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Division of Synchrotron Radiation Research

Department of Physics

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Front cover: Artistic interpretation of the normalized differential conductance along a contacted GaSb-InAs nanowire.

Back cover: Slightly bent W-tip.

Division of Synchrotron Radiation Research
Department of Physics
Lund University

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"I'd like to congratulate myself, and thank myself,
and give myself a big pat on the back"
– Dee Dee Ramone

Abstract

This dissertation presents the new methods and techniques developed to investigate the properties of nanowires (NWs) and NW devices and the results obtained using these methods. The growth and characterization of NWs have become a large research field because NWs have been shown to improve the properties of many semiconductor applications such as transistors, solar cells, and light emitting diodes. The structural composition, optical properties, and electric characteristics of NWs and NW devices are affected by effects at the atomic level. The surface of NWs plays a crucial role when it comes to these characteristics because of the large surface to volume ration of the NW structures. This makes the characterization of these structures, at the atomic level, a key factor, for understanding the underlying mechanisms, and for the development of even more suitable structures. Here, the composition of III-V semiconductor materials and the electronic properties of III-V semiconductor NWs are investigated using scanning tunneling microscopy (STM) and X-ray photoelectron spectroscopy (XPS).

A new method for studying contacted NWs on insulating substrates with STM is described, and the results from investigations of InAs-GaSb Esaki diode NWs are presented. The ability to study the NW side facets with STM while at the same time being able to apply a potential along the NW makes it possible to connect the device performance with the NW characteristics found with the STM.

The conductivity of up-standing, as-grown NWs is also measured with an STM using the novel technique called top contact mode. The method is used to evaluate, the Schottky barrier height of the Au-GaAs interface in GaAs NWs, and the conductivity of InP and InAs NWs. This method makes it possible to measure the electric conductivity of the NWs without any additional device fabrication, making it more reliable due to the good ohmic electrical contacts established to the NW. It also, in contrast to conventional methods, enables well-controlled surface treatment of the NW side facets which is used to show how surface oxides influence NW conductance.

XPS and the more penetrating hard X-ray photoelectron spectroscopy (HAXPES) are used to evaluate the homogeneity and the growth of HfO_2 films on InAs as well as the mechanism behind the self-cleaning effect of the InAs native oxide.

This information is especially important for the continued work on semiconductor transistors where the HfO_2 is one of the best candidates to be used as the gate oxide and where the interface between the oxide and semiconductor is crucial for device performance.

Populärvetenskaplig sammanfattning

Nanoteknik är i grunden förmågan att kunna påverka material ner på dess mest grundläggande nivå, d.v.s. atomär nivå. Ett sådant vitt begrepp gör att väldigt mycket kan beskrivas som nanoteknik vilket i sin tur kan medföra en del förvirring kring vad nanoteknik egentligen är. Ett sätt att se på det är helt enkelt att nanoteknik är en del av den naturliga utvecklingen av naturvetenskapen där ökad förståelse leder till mer precisa verktyg som i sin tur leder till ökad förståelse och så vidare. Själva ordet nano syftar till nanometer vilket i sin tur betyder miljarddels meter. Som jämförelse har en vanlig hudcell en diameter på ungefär 30000 nanometer. På en nanometer får c:a tre atomer i rad plats.

Halvledare är material som leder ström, fast dåligt. Deras ledningsförmåga kan dock påverkas permanent genom s.k. dopning där orenheter tillförs materialet, eller tillfälligt genom att utsätta halvledarna för elektriska fält. Dessa egenskaper visade sig vara perfekta för utvecklingen av elektriska komponenter och halvledarmaterialen är grunden till bl.a. lysdioder (populärt kallat LED-lampor) och många sorters solceller. Halvledarmaterialens egenskaper är också en av de grundläggande orsakerna till att datorutvecklingen tog sådan fart som den gjorde. Genom att byta ut de klumpiga radiorören som användes i dåtidens datorer mot transistorer gjorda av halvledarmaterial kunde flera fördelar uppnås. Datorerna blev driftsäkrare, de blev mindre, drog mindre ström och framförallt kunde de utföra beräkningar snabbare. Antalet transitorer i en dator är direkt kopplat till hur snabb den är. Genom att göra transistorerna mindre och mindre (så att antalet i en dator ökar) så kan allt snabbare datorer tillverkas. Det är denna förminskning som har drivit datorutvecklingen i mer än ett halvt århundrade men nu är transistorerna så små att de inte kan bli mycket mindre. Problemet är att när vi kommer ner på nanonivån så börjar material uppföra sig annorlunda än vad vi är vana vid, de får andra egenskaper. Elektroner börjar tunnla, vilket innebär att strömmar kan uppstå där de klassiskt sett inte skulle kunna finnas. För att beskriva vad som händer kan man inte längre förlita sig till den klassiska fysiken utan istället måste kvantfysikens lagar tas i beaktning. För att föra utvecklingen framåt kan vi då istället vända på problemen som uppstår på nanoskalan och använda de nya förutsättningarna till vår fördel. För att kunna göra det krävs en ökad förståelse och det är där som vår forskning kommer in i bilden.

I den här avhandlingen beskrivs den forskning vi har bedrivit för att öka förståelsen kring vad som händer med halvledarkomponenter när de krymps ner till nanoskalan. Mycket fokus har lagts på att utveckla verktyg och metoder med vilkas hjälp experiment kan utföras. De två huvudsakliga verktygen har varit svepspetsmikroskopi och fotoelektronspektroskopi med vilka speciella strukturer kallade nanotrådar i huvudsak har undersökts. Nanotrådarna vi har undersökt är små pinnar gjorda av halvledarmaterial som är runt 1 μm långa (dvs i storleksordningen som en bakterie, och mycket mindre än en mänsklig cell). Med rätt förhållanden kan man få nanotrådar att växa på halvledarplattor bara man tillför rätt gaser vid rätt temperatur och tryck. Genom noggranna beräkningar och experiment kan man styra hur nanotrådarna växer. Det går att skapa alla möjliga strukturer, med atomär precision, t ex solceller, lysdioder eller transistorer.

Vi har utvecklat en ny metod att använda svepspetsmikroskopi för att undersöka ytan hos nanotrådar medan de har varit utsatta för olika elektriska spänningar. Vi har även utvecklat en annan metod för att kontaktera nanotrådar och mäta hur strömmen varierar genom dessa beroende på vilken elektrisk spännig de utsätt för. Båda metoderna har utvecklats för att det behövs mer kunskap om hur, och framför allt varför, nanotrådar beter sig som de gör.

Fotoelektronspektroskopi har framför allt använts för att belysa frågor kring hur tunna oxidlager kan skapas och hur deras sammansättning ser ut. Dessa oxidlager spelar en framträdande roll i utvecklingen av morgondagens transistorer.

Preface & List of papers

This doctoral thesis presents my contribution to our work on developing new and utilizing existing techniques to evaluate nanowires and nanowire devices over the last five years. Here, the techniques and methods developed during this time span are explained. The underlying theory is presented as well as the results which have been published in scientific journals. Parts of this work have previously been presented in my licentiate thesis "Surface studies of III–V nano devices". This doctoral thesis is based on the following papers, which will be referred to in the text by their Roman numerals.

Paper **I**

Scanning Tunneling Spectroscopy on InAs–GaSb Esaki Diode Nanowire Devices during Operation

O. Persson, J.L. Webb, K. A. Dick, C. Thelander, A. Mikkelsen, and R. Timm

Nano Letters, **15**, 3684 (2015)

I was involved in the planning of the experiment and responsible for the development of the techniques used as well as the measurements. I analyzed the data and wrote the manuscript.

Paper **II**

High Resolution Scanning Gate Microscopy Measurements on InAs/GaSb Nanowire Esaki Diode Devices

J. L. Webb, O. Persson, K. A. Dick, C. Thelander, R. Timm, and A. Mikkelsen

Nano Research, **7**, 877 (2014)

I was involved in the planning of the experiment as well as the measurements and I took part in the discussions about the manuscript.

Paper **III**

Current–Voltage Characterization of Individual As-Grown Nanowires using a Scanning Tunneling Microscope

R. Timm, O. Persson, D. L. J. Engberg, A. Fian, J. L. Webb, J. Wallentin, A. Jönsson, M. T. Borgström, L. Samuelson, and A. Mikkelsen

Nano Letters, **13**, 5182 (2013)

I was involved in the planning of the experiment, measuring the data, and development of the technique. I analyzed parts of the data and contributed to writing the manuscript.

Paper **IV**

The Effect of Surface Oxide and Wurtzite/Zinc blende Interfaces on the Conductivity of InAs Nanowires

O. Persson, L. Kral, S. Lehmann, C. Thelander, A. Mikkelsen, and R. Timm

In manuscript

I was involved in the planning of the experiment and responsible for the measurements. I analyzed the data and wrote the manuscript.

Paper **V**

Strong Schottky Barrier Reduction at Au–Catalyst/GaAs–Nanowire Interfaces by Electric Dipole Formation and Fermi-level Unpinning

D. B. Suyatin, V. Jain, V. A. Nebol'sin, J. Trägårdh, M. E. Messing, J. B. Wagner, O. Persson, R. Timm, A. Mikkelsen, I. Maximov, L. Samuelson, and H. Pettersson

Nature Communications, **5**, 3221 (2014)

For the nanowires described as series B, I was involved in the planning of the experiment, measuring the data, and development of the technique. I analyzed the data for series B and took part in discussions about the manuscript.

Paper **VI**

Interface Characterization of Metal–HfO_2–InAs Gate Stacks using Hard X-ray Photoemission Spectroscopy

O. Persson, E. Lind, E. Lundgren, J. Rubio-Zuazo, G. R. Castro, L.-E. Wernersson, A. Mikkelsen, and R. Timm

AIP Advances **3**, 072131 (2013)

I was involved in the planning of the experiment as well as the measurements. I analyzed the data and wrote the manuscript.

Paper **VII**

Self-cleaning and Surface Chemical Reactions during HfO_2 Atomic Layer Deposition on InAs

R. Timm, A. Head, S. Yngman, J. V. Knutsson, M. Hjort, S. McKibbin, A. Troian, O. Persson, S. Urpelainen, J. Knudsen, J. Schnadt, and A. Mikkelsen

In manuscript

I took part in the measurements and discussions about the manuscript.

Abbreviations and Symbols

III-V	material comprised of one group III-element and one group V-element in the periodic table
A*	Richardson constant
AHC	atomic hydrogen cleaning
ALD	atomic layer deposition
APT	atom probe tomography
APXPS	ambient pressure X-ray photoelectron spectroscopy
Å	angstom
CB	conduction band
CBE	conduction band edge
CMOS	complementary metal oxid semiconductor
CU	controler unit
E_i	energy, initial state
E_F	Fermi energy
E_f	energy, final state
E_G	band gap energy
E_K	kinetic energy
EDX	energy dispersive X-ray spectroscopy
ESRF	European synchrotron radiation facility
FET	field effect transistor
H*	atomic hydrogen radical
HAXPES	hard X-ray photoelectron spectroscopy
I_S	saturation current
IMFP	inelastic mean free path
I_T	tunneling current
K	decay length
LDOS	local density of states
LED	light emitting diod
$M_{i,f}$	tunneling matrix element
MBE	molecular beam epitaxy
MOSFET	metal oxide semiconductor field effect transistor
MOVPE	metal organic vapor phase epitaxy

NW	nanowire
SEM	scanning electron microscope
SGM	scanning gate microscopy
SPM	scanning probe microscopy
STM	scanning tunneling microscope/microscopy
T	tunnel probability
T_C	congruent evaporation temperature
TEM	transmission electron microscope
UHV	ultra high vacuum
VB	valence band
VPE	vapor phase epitaxy
VT	tip bias
XPS	X-ray photoelectron spectroscopy
ϵ_0	vacuum permittivity
κ	relative dielectric constant
λ	inelastic mean free path
ϕ	work function
ϕ_{bi}	built in potential
ϕ_{Bn}	barrier height
χ	electron affinity

Acknowledgements

There are of course many people who have helped and guided me in my work during the timespan of this thesis, and I hope that I remember to acknowledge you all.

First of all, I would like to thank my supervisor, Anders, for all your support and positive attitude to my various ideas, and also of course for everything you have taught me. I can not stress enough how glad I am that I have had such a positive and encouraging supervisor. Also, your ability to make sense of even the most convoluted and confusing manuscripts I've written so that other people also can understand them is much appreciated.

My co-supervisor Rainer with whom I even shared an office when I started at the division. You have such an approachable and kind personality. You are most probably the person who has taught me most about all the various experimental techniques and the theory behind them. We have also been on many beam-times together, and I must thank you for all of your candy that I have eaten. You have also been a tremendous help when it comes to my writing and presenting material at various conferences.

Martin and Johan, you have taught me everything I know about practical STM work (except for everything Anders and Rainer taught me), thank you. You, together with Erik M., are for sure the silliest physicists I know, keep it up.

There have been students helping me these past five years. Jalil, Jovana, and Lena, you all kept on working even though it did not always go according to plans.

Thank you Estephania. If something is broken, one can always count on your help.

Everyone else who has been in the STM labs working with me, thank you.

All my former office mates, Erik M., Elin, Natalia, Olesia, Erik M., Sophie, Chu chu, and Andrea. We have shared many laughs, disappointments, and stories.

Thank you, Sara. I think discussing things, not necessarily strictly connected to surface science all the time, is a good way of not losing track of what is important here in life.

Patrik, thank you for all the support related to me getting money from the university. You have helped a lot. And also, thank you for your stories and gossip.

It has been great fun and very educational working together with you, Elisabeth. I think we have shared many eureka moments, teaching these last five years.

The I311 people and especially Karina. I do not want to recall all the phone calls I have made in the middle of the night to you guys. Thank you for being so understanding and helpful.

Electrical measurements, device fabrication, and general STM/AFM stuff, thank you, Jim, I've learned a lot.

None of my work would have been possible without samples to investigate. Thank you, Claes, especially for your very interesting Esaki diodes that really helped us when starting with the STM on device-measurements. Thank you, Kristian and Sebastian, as well for the various samples that we have destroyed. The collaboration with Lars-Erik and Erik and the rest of your group with all the NW-wrap gate related samples.

All the people at solid state physics and especially the clean room staff for all the equipment training.

I also have to thank the rest of my co-workers at the department of synchrotron radiation research. I strongly feel that there are a community and warmth at the division which may not be that common in the research world. Keep it up.

Writing this thesis would not have been possible if it was not for my parents and my in-laws and all the help with taking care of Stina afternoons and evenings. Thank you.

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Contents

1 Introduction

It is hard to imagine how our modern world would look without the use of semiconductor materials. The fact that a modern computer now fits in your hand (smartphone) is all thanks to semiconductors. A computer consists, at its core, of billions of small semiconductor devices called transistors. Semiconductors are also the key material in solar cells, light-emitting diodes (LEDs) and many other applications today.

During the timespan of this thesis I have, together with my colleagues and collaborators, studied the properties of semiconductor devices at the nanoscale. Nanoscience is the description and understanding of the novel properties that different material systems exhibit when they are shrunk into the nanometer (nm) scale. These new properties give rise to semiconductor devices with completely new scopes. Due to the small dimensions of these structures, classical physics are not enough to describe their electronic properties. The laws of quantum mechanics have to be taken into account to be able to explain and understand how and why they work. The laws of quantum mechanics state that all matter can mathematically be described, not only as particles but also as waves, and that classical physics is in fact merely a statistical result of quantum mechanics, at larger scales.

There are however many challenges associated with the making of nanoscale semiconductor devices. For example, at the atomic level, it is almost inevitable not to get imperfections at the interface between different materials which will deteriorate the performance of many devices. A very promising semiconductor material shape called the semiconductor nanowire (NW) has been shown to circumvent many of these challenges, and it has also been shown to improve upon the performance (switching speeds of transistors, efficiency of solar cells and LEDs) of many semiconductor devices when integrated as an active part.

In this thesis, I have focused on revealing and understanding the properties of semiconductor NW structures and some of their applications, solar cells, LEDs, and transistors. To do this new methods and techniques had to be developed to enable us to couple the atomic structure of NWs with their electronic behavior. Much focus has been put into investigation of individual NWs and the development of techniques to enable us to couple the individual NW surface

structure with the NW electrical characteristics. The mere fact that NWs are so small in size makes this challenging.

The two main techniques used to conduct the research presented in this thesis are scanning tunneling microscopy (STM) and X-ray photoelectron spectroscopy (XPS). Both are so-called surface sensitive techniques highlighting the fact that they only analyze the outmost atomic layers of the sample studied. Using various methods and tricks, we utilize these surface sensitive techniques to also, in various ways, probe deeper into our samples to reveal further information.

In this introduction chapter, an overview of the semiconductor world will be given with a focus on the areas which are most important for my research.

1.1 III–V semiconductors

All the results presented in this thesis are from research and experiments on III–V semiconductor material. Semiconductor materials have higher electrical conductivity than insulators but lower than metals. This property in itself did not make semiconductor materials especially interesting from an electronic device maker's point of view, but it was the ability to change the conductivity in a controlled manner of these materials by introducing minute amounts of other materials, so-called dopants, that did [1].

The predominantly used material in the semiconductor industry was, in the beginning, Ge which later got replaced by Si [2]. One of the major reasons for the replacement is because Si naturally forms a thin layer of insulating SiO_2 which is stable and can have very few interface defects which are highly useful in the industry. The increasing demand for faster electronics and more efficient LEDs and solar cells has led to a demand for materials with more suitable properties. New semiconductor materials are needed with different band gap size, charge carrier mobility, carrier generation and recombination, and direct or indirect band gap. Both Ge and Si are from the fourth group of the periodic table. By combining materials from the third and fifth group in the periodic table new semiconductor materials become available, hence the name III–V semiconductors. These materials can then be designed so that they satisfy many of the desired properties.

The use of III–V semiconductors has two main reasons. In the case of transistors, it is the high charge carrier mobility which makes them ideal for high switching speeds [3]. For LEDs, it is the direct band gap of many III–V semiconductors [4] which allows for fast electron-hole recombination and thereby good electricity-to-light efficiency, and vice versa for solar cells. By using more than one element from group three and group five and controlling the ratio between the same (e.g. $Ga_xIn_{1-x}As_yP_{1-y}$), tailoring of the band gap and lattice constant of the resulting material is possible.

The use of III–V semiconductors in the industry is limited, especially in the complementary metal oxide semiconductor (CMOS) industry where Si still is the predominant material [5]. The technology needed to use III–V semiconductor materials is less explored and thereby more expensive than the standard Si technology. The materials themselves are more expensive, and the integration with the Si technology is challenging due to the distinct differences in the industrial processing of Si and III–V semiconductors [6]. When combining Si and III–V semiconductors, anti-phase domains can arise which leads to the formation of defective material. The different domains are created when III–V semiconductor

material growth is initiated on two different Si atomic planes with only one atom in height difference [7]. Where the domains meet defects arise.

The difference in lattice constant (physical dimensions of the smallest unit cell of a crystalline material) between most III–V semiconductors and Si also creates integration problems. A difference in lattice constant between two materials will lead to strain in the interface between the same, which in turn leads to dislocations which will deteriorate the performance of most devices made this way. The lattice constant of the semiconductor at the interface to the Si can, in some cases, be tailored to match the lattice constant of Si. There is, however, an additional problem with integration between Si and III-V semiconductors, and that is the difference in the coefficient of thermal expansion. Two materials with different coefficients will expand or contract to different degrees when exposed to temperature variation which will also lead to dislocations at the interface between the two materials.

By growing semiconductor nanowires (NWs) – self-assembling, rod-shaped structures – many of these limitations can be overcome, and the realization of more complex III–V semiconductor-Si devices can be realized [8, 9]. Typical NWs have a width of 10 to 100 nm and a length of 1 to 10 μm. NWs can accommodate the strain caused by growing materials with different lattice constants due to the small cross-section area and by effect large surface to volume ratio. The surface of the NW accommodates the strain caused by the lattice mismatch at the NW–substrate interface, allowing an elastic deformation to take place with no dislocations forming at the interface. This enables NWs to handle much more strain than an ordinary bulk structure of the same materials could. Since NWs grow separately from each other, there will never be any domains with different phases. Thus, they are ideal for implementing III–V materials with Si technology [7, 10].

1.2 Semiconductor doping

Doping plays a crucial role when it comes to semiconductor device production and operation. Doping is the process of introducing impurities into a semiconductor material resulting in either an excess of electrons or holes. Epitaxially grown semiconductor materials without any *added* impurities are said to be nominally undoped (or intrinsically doped), because a small amount of dopants will always be present. Introduced dopant atoms exchange position with an atom in the semiconductor lattice. The dopant either has less (acceptor) or more (donor) valence electrons compared to the substituted atom. Donors create an excess of electrons in the semiconductor (*n*-doping), fig 1.1(a), and acceptors

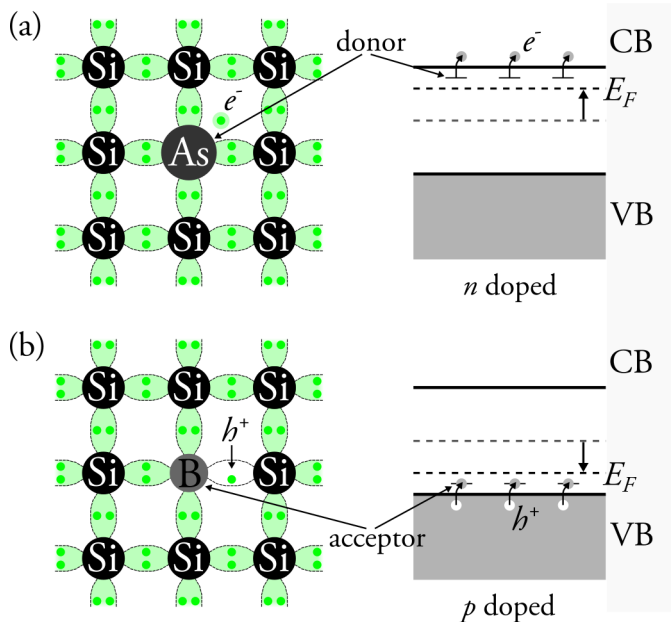

Figure 1.1: Schematic representation of doping of semiconductors. (a) *n* doping of Si with As. The As atom has five valence electrons, one too much to fit in the Si lattice. The extra electron is "donated" to the Si conduction band, raising the Fermi level. (b) *p* doping of Si with B. The B atom, on the other hand, has only three valence electrons, one too little to fit in the Si lattice. The B "accepts" an electron from the Si, creating a mobile hole in the Si valence band, lowering the Fermi level.

create an excess of free electron holes (*p*-doping), fig 1.1(b). Dopants have an energy level which either lies just beneath the conduction band (donor) or above the valence band (acceptor). The energy difference between the dopant level and the band edge is typically so small that, at room temperature, the dopants are ionized.

The crucial role of doping in device making is that it shifts the Fermi level (the hypothetical energy level that has a 50% chance of being occupied by an electron, at thermal equilibrium) of the semiconductor. By introducing electron states close to the conduction band, the Fermi level is raised in that material and vice versa, fig 1.1. In thermodynamic equilibrium, the Fermi level of a system has to be constant which means that the valence- and conduction band of differently doped semiconductors have to bend if brought into contact with each other. This is utilized in almost all semiconductor devices, fig 1.2.

1.3 Surfaces

The properties of the surface of a material are in some cases more important and interesting than the properties of the bulk of the material. Heterogeneous catalysis is a classic example. It is a process where a chemical reaction is facilitated between reactants in one phase by a catalyst in another. Typically the reactants are in gas or liquid phase, and the catalyst is in solid phase. For a solid catalyst, it is only the outermost atoms of the whole catalyst material that are interesting. It is only these atoms and their properties that govern the mechanisms involved in the catalytic reaction.

In electronics devices based on crystalline materials, the surfaces are seen as irregularities. In the ideal case of an infinite, periodic crystal, the electrons have well defined allowed energy bands. A surface of a material breaks this periodicity in one dimension giving rise to new energy states which are allowed in that dimension. The notion of an infinite crystal is, of course, absurd in real life, but the approximation holds for most crystals since the number of bulk atoms in relation to surface atoms is so large. The bulk states outnumber the surface states to such a degree that the surface states effects are negligible. At the nanoscale, though, this approximation breaks down as the ratio between bulk and surface atoms gets smaller and smaller when shrinking the size of the devices. This is one of the major challenges when trying to understand and design nanoscale devices since the smaller you make your device, the more your material properties will be determined by surface effects and differ from the properties of the same material in bulk form. At the surface of crystalline materials, the atoms can change their arrangement compared to the bulk to lower their potential energy. This is called reconstruction. The unit cell of a stable surface reconstruction of Si(111), imaged with an STM in 1983 by G. Binnig et al. [11], is, for example, seven times longer and much more complex than the unit cell of the bulk structure.

Since the surface plays such a large part when it comes to determining the properties of material at the nanoscale, it is of utmost importance to be able to investigate and characterize surfaces and their properties. Once understood, the effects of the surface properties can not only be minimized but potentially utilized to give rise to new material properties which are then also structure based.

1.4 Basic devices

The applications in which III–V semiconductor materials are utilized to improve the performance are growing every year. Our research is focused on increasing the understanding of how and why these new applications work. There are three general types of semiconductor devices which demonstrate the basics for these applications. The devices are: 1) the light emitting diode (LED), 2) the photovoltaic cell, commonly named solar cell, and 3) the transistor. The basic working principles for these devices will be described in this section.

The building block of all these devices is the *p*–*n* junction which consists of two differently doped parts where one (*n*) has an excess of free electrons, and the other part (*p*) has a deficit. At the junction between these parts, the electrons will diffuse from the *n*-part with an excess of electrons into the *p*-part, creating a so-called depletion region. This will create a local electric field (the built-in potential) over the depletion region which in turn will facilitate any flow of electrons through the *p*–*n* junction in the *p*-to-*n* direction.

In fig 1.2 the band diagram of the central area of an LED, a solar cell, and a metal oxide semiconductor field effect transistor (MOSFET) are depicted. A band diagram is a simplification in two dimensions showing the allowed energies for the electrons in the specific system. An ideal semiconductor (at 0 K) has two bands which are important for its electronic behavior, the valence- and conduction band, with energy states electrons can occupy. Between these two bands, there is the band gap without any allowed energy states. The energy states in the valence (lower) band are all filled, and all the states in the conduction (top) band are empty. Since all the states are occupied in the valence band, the electrons can not move, and no flow of electrons (electric current) is possible. For an electrical current to be possible, an electron first has to occupy a state in the conduction band. This can be done by absorbing energy, typically from heat (if the temperature is above 0 K), or from incoming light.

The *p*-*n* junction is the most important part in both the LED, fig 1.2(a), and the solar cell, fig 1.2(b). In the LED, a potential is applied across the *p*-*n* junction, and charge carriers (negative electrons or positive electron holes) flow into the depletion region where a fraction of the electrons and holes recombine, emitting photons. The efficiency of the LED (luminous efficacy: the ratio of luminous flux to power) depend on the amount of charge carriers that recombine and emit a photon, and it can be up to one order of magnitude higher than for standard incandescent light bulbs [12]. The emitted photons from an LED will have the

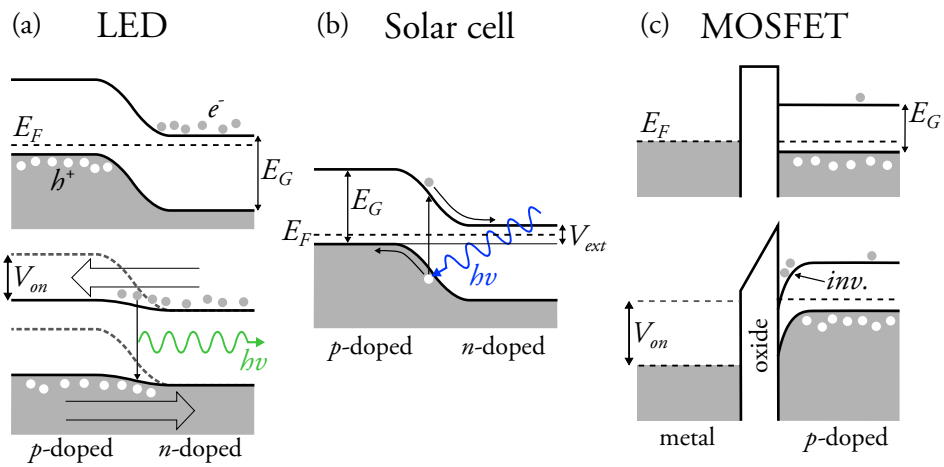

Figure 1.2: Energy band diagrams of three common (idealized) semiconductor devices. In (a) the LED is shown. By applying a bias (V_{on}), the built-in potential of the depletion region is counteracted, and the electrons e^- and holes h^+ can diffuse into the depletion region and recombine emitting photons with energy hv corresponding to the band gap energy E_G. In (b) a solar cell is shown. Electrons are excited by incoming photons, with energy $hv > E_G$, creating electron–hole pairs. The charge carriers are accelerated by the built-in potential, in the depletion region, and reach the contacts on either side. The highest theoretical bias that can be extracted (V_{ext}) from a single *p*-*n* junction is equal to the difference between the conduction band edge at the *n*-contact and the valence band edge at the *p*-contact. Greater bias can be achieved by connecting several solar cells in series. In (c) a metal oxide semiconductor field effect transistor (MOSFET), in this case with a *p*-doped channel, is shown. A positive potential at the metal gate (V_{on}) will lead to an inversion layer of electrons in the semiconductor at the interface to the gate oxide. This creates a conducting layer between the *n*-doped source and drain, turning the transistor "on".

energy, hv, corresponding to the band gap energy, E_G, of the semiconductor material from which it is made, fig 1.2(a). An LED made of one single semiconductor material will hence emit light with a highly defined wavelength. For lighting applications where white light, with high color rendering index, is required this is far from ideal. LED-lamps bought in stores today solve this problem by using a blue LED in combination with a phosphorous coating, known as YAG, which absorbs some of the blue light and emits yellow through fluorescence [13]. This will produce white light with low color rendering index. With careful engineering using more complex designs than the standard *p*–*n* junction and different semiconductor materials, LEDs with higher color rendering index can be achieved [14]. These LEDs are able to emit photons with wavelengths in both the blue, green, and yellow spectra which also give the LEDs a higher luminous efficacy since they do not lose any energy from conversion in the YAG coating.

The photovoltaic cell is in many ways the opposite of the LED. Instead of generating photons via electron–hole recombination, electron–hole pairs are generated via absorption of photons. A photon with energy $h\nu > E_G$ can excite an electron from the valence band into the conduction band. These charge carriers, if generated in the depletion region, are then separated by the built-in potential creating a flow of charges, an electric current, fig 1.2(b). Here the different material properties of III–V semiconductors, as well as more elaborate designs, can also be utilized to construct more efficient photovoltaic cells [15, 16]. A solar cell comprised of a single semiconductor material will absorb photons with energies $h\nu > E_G$ but all the energy above E_G will be lost as heat as the electron relaxes down to the conduction band edge. Also, all photons with energies $h\nu < E_G$ will not be absorbed. By combining semiconductor materials with different band gaps, this problem can be circumvented to a larger degree, and the wide spectrum of photon energies in the sun light can be harvested more efficiently.

Arguably the most important electronic component today is the transistor. A transistor can be built in many ways, but they are all constructed to amplify an electric signal. By connecting transistors in clever ways, logic gates and in turn whole processors can be constructed. The transistors work because it is so easy to manipulate the amount of charge carriers in doped semiconductors. By applying a small bias to a controlling gate, the conductance of a channel between the source and drain of the transistor can be changed dramatically. This is the amplifying behavior behind most transistors. In a processor, current between a source and a drain is a logic *one*, and no current is a logic *zero*. The basic principle of the metal oxide semiconductor field effect transistor (MOSFET) is shown in fig 1.2(c). The gate (metal) is separated from the *p*-doped semiconductor channel with an oxide; the *n*-doped source and drain are not shown in fig 1.2(c). In this sketch, they are situated behind and in front of the image. By applying a positive bias to the gate, electrons will accumulate in the conduction band of the semiconductor at the interface to the oxide, forming an inversion layer. The inversion layer has the same type of charge carriers as the source and drain (in this case electrons), allowing for a current to flow between the same. The MOSFET can have either a *p*-doped channel (nMOS) or an *n*-doped (pMOS). The pMOS works just as an nMOS, but everything is opposite, one applies a negative bias to create an inversion of holes. These two kinds of transistors are then combined forming the complementary metal oxide semiconductor (CMOS) technology which is the backbone of modern integrated circuits design.

1.5 Aim and outline of this thesis

In this doctoral thesis, new methods developed by us for investigations of NWs and NW devices will be presented together with the underlying theories and principles. These methods were developed because there is a need for more information and a better understanding of NWs to enable further development of semiconductor NW devices. The aim is to increase our knowledge and explain, what is happening at the atomic level.

The thesis is based on seven publications which can be divided into two groups with respect to the main technique used. In Papers **I**–**V** STM, located in Lund at the division of synchrotron radiation, has been used, often in unconventional ways, to obtain both structural and electronic information from different III–V semiconductor devices. In Paper **VI** and **VII** photoelectron spectroscopy techniques, placed at the synchrotrons in Grenoble (ESRF) and Lund (MAX-lab), respectively, have been used to obtain structural and chemical information from different III–V semiconductor devices.

In Paper **I** a combined atomic force microscope/STM is used to study a contacted III–V semiconductor NW during operation for the first time. In Paper **II** the same combined microscope used in Paper **I** is here utilized to perform high resolution scanning gate microscopy on a contacted semiconductor NW. Paper **III** explains the novel technique of using an STM for contacting up-standing NWs directly. This technique is then utilized in Paper **IV** to determine the conductivity of InAs NWs with crystal structure interfaces. The influence of the presence of a surface oxide on the NWs is also studied. The same technique is also used in Paper **V** to determine the Schottky barrier height between InAs NWs and their Au seed particles. In Paper **VI** hard X-ray photoelectron spectroscopy is used to study a stack with HfO_2 deposited with ALD on InAs with a top layer of metal. The influence of the metal and the composition of the HfO_2 are examined. Paper **VII** uses the results found in Paper **VI,** but here time-resolved X-ray photoelectron spectroscopy is used to analyze the growth of the HfO_2 layer in detail.

The thesis consists of two parts where the first covers the theoretical background and gives an introduction to the different experimental techniques used in the articles presented in the second part. The first part is divided into four chapters. In chapter 1an introduction to the research field was given. In chapter 2 NWs and how these can be made into semiconductor devices are explained. Chapter 3 then contains all the experimental technique used and developed for our research. The STM is explained in detail and how it can be utilized to also investigate NW devices and measure the conductance of as-grown NWs. Here X-ray photoelectron

spectroscopy (XPS) is also described, and the advantages of hard X-ray photoelectron spectroscopy (HAXPES) are discussed as well as ambient pressure X-ray photoelectron spectroscopy (APXPS). Finally, chapter 4 summarizes and concludes the thesis and also gives an outlook on the future of our research field.

2 Nanowire devices

All the NWs studied in this thesis are III–V semiconductor NWs. Despite their name (wires) they are perhaps more correctly described as elongated rods with the typical width of 10 to 100 nm and length of 1 to 10 μm, fig 2.1. The III-V semiconductor NWs are crystalline objects, the atoms in the NWs are arranged in an ordered structure with a repeating pattern. The structure can be described using the atoms that make up the smallest unit in this pattern called the unit cell. The parameters describing the unit cell are referred to as the lattice parameters, and they describe the length of the principal axes of the unit cell and the angles between these. If the width of a NW is small enough the NW can be considered to be a one-dimensional structure where the energy levels of the electrons are quantized in two dimensions. This minimum width for quantization is dependent on many factors such as the NW structure, the NW material, the temperature, and the de Broglie-wavelength of the electrons (0.1 nm in metals but up to 40 nm for semiconductors). The NWs studied during the work presented in this thesis are however large enough not to show this behavior, typically 100 nm in width.

The focus on III–V semiconductor materials in the shape of NWs has been brought on for several reasons. The small width of the NWs allows for strain relaxation in the radial direction which enables change in material composition along the axis between materials of highly different lattice parameters without the formation of stacking faults [17, 18]. The structural and optoelectrical properties of NWs may also be different from the corresponding bulk material [19]. NWs have been shown to improve the performance of electronic devices mentioned in chapter 1 such as LEDs [20-23], photovoltaic cells [24-28], and transistors [29-31]. Also in life science, many applications have been shown [32, 33]. The high surface to volume ratio of NWs is as well advantageous when constructing sensors [34, 35].

In fig 2.1 two scanning electron micrographs of different InP NWs are shown. Here the typical elongated rod shape is seen as well as the Au seed particle on top of the NWs which is used to catalyze the growth. These NWs, as well as all the NWs investigated throughout this thesis, are made with a bottom-up technique, usually referred to as NW growth.

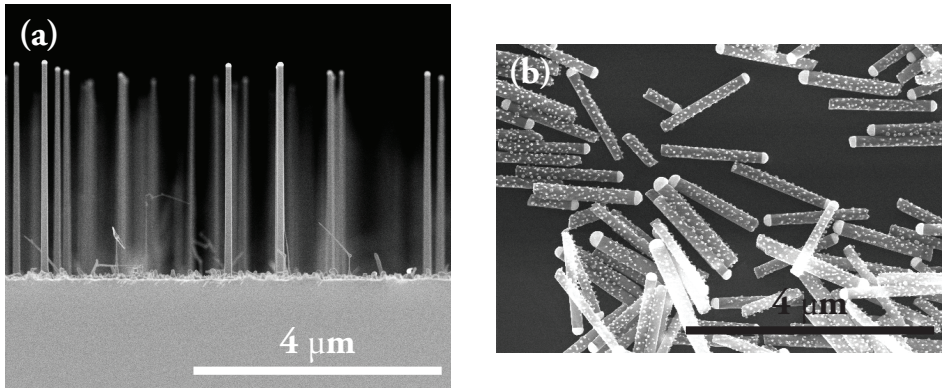

Figure 2.1: Two scanning electron micrographs of two different samples of InP semiconductor NWs grown with Au seed particles. The image in (a) was recorded in cross-section with the NWs standing as-grown on the InP substrates. In (b) a different set of NWs are shown. The NWs have been broken of their growth substrate and put on a new substrate to enable STM investigations of the NW side facets. Here the image was recorded after several heat treatments, and undesired droplet formation (due to excessive heating) is seen on the NW side facets. Images (a) is courtesy of J. Wallentin.

2.1 Nanowire growth

Traditionally in the semiconductor industry, devices have been constructed using top-down methods; features down to the nm-scale are etched out, using lithographical processes, of larger blocks in many step processes [36]. There are a great variety of methods used to make NWs, the top-down techniques where you etch away material to form NWs and the two main bottom-up: Solution-phase synthesis and vapor phase epitaxy (VPE). With bottom-up techniques, NWs self-assemble into a wanted structure, given the right circumstances. The process is known as NW growth.

In solution phase synthesis, nanostructures are grown in a high-purity supersaturated melt, and it can be used to grow e.g. Si or Ge homogeneous NWs [37]. It is a more simple method than VPE but it also has the limitations when it comes to material compositions, as well as structural design. For growth of III-V semiconductor NWs, VPE is most commonly used [38] due to the fact that there are more precursors in the vapor phase available, and the control of said precursors can be extremely precise, allowing for atomically sharp interfaces between different materials to be made. The two main techniques for VPE are molecular beam epitaxy (MBE) and metal-organic vapor phase epitaxy (MOVPE).

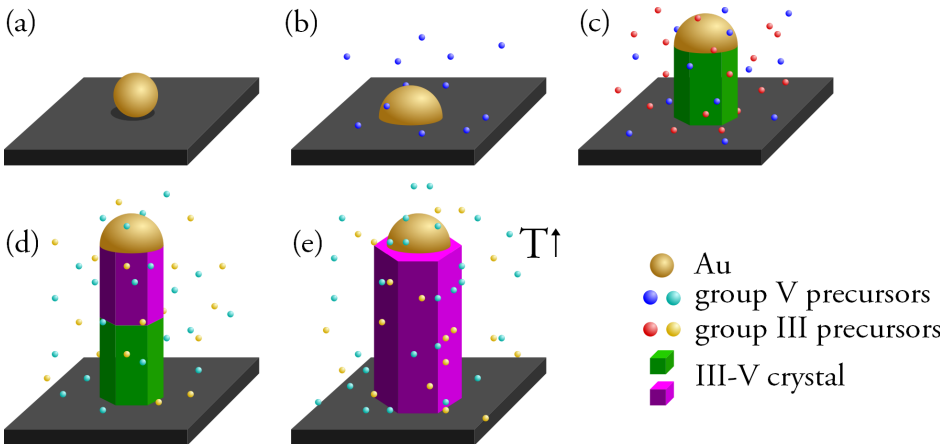

Figure 2.2: Au-particle-assisted NW growth in a schematic view. (a) Au particle is deposited on a substrate. (b) Annealing under group V precursor pressure to remove native oxide. (c) Group III precursor is applied, supersaturation of Au particle leads to NW growth. (d) Axial heterostructures can be formed by changing precursors. (e) Introducing radial growth by increasing temperature.

Growth with MBE is done under ultra-high vacuum (UHV) pressures below 10^{-9} mbar. The growth constituents are supplied to the growth substrate via elemental beams. Since MBE is performed in UHV the elements travel to the growth substrate without interacting. Once at the substrate, they condense and can interact with each other. MBE can be very precise, and the set-up itself is cheaper than MOVPE. The big drawback for industrial application is the slow growth speed which makes the production cost of mass production of NWs much higher. In the industry, the desired approach would be to produce NWs with MOVPE [38].

All NWs studied in this thesis are grown with MOVPE using Au-particle-assisted growth on crystalline substrates. Epitaxial NW growth is an atomic layer-by-layer growth forming a crystal with the same crystal orientation as the growth substrate. One typically distinguishes between homo- and heteroepitaxy where the former indicates that the NW grown is of the same material as the growth substrate and the latter that it is a different material.

In MOVPE a carrier gas, H_2 or N_2, is used to transport the growth precursors to the growth substrate. The group III precursors are typically metal-organic compounds such as trimethylgallium ($Ga(CH_3)$) and the group V precursors are hydrides such as arsine (AsH_3). The precursors decompose and form crystalline III-V semiconductor material while the organic ligands react with the hydrogen and are desorbed. Au-particle-assisted NW growth starts with the deposition of Au particles on a crystalline growth substrate with a certain crystallographic direction, typically <111>B, fig 2.2(a). The substrate is then annealed in the MOVPE

growth chamber to remove unwanted contaminants and the native oxide of the substrate, fig 2.2(b), under group V precursor overpressure. This also melts the Au particles. The group III precursor is then also applied and alloys with the Au particle. At a certain point, the Au particle becomes supersaturated, and there will be a nucleation of III-V material between the Au particle and the substrate. More precursors are continuously supplied, and the deposition of material continues under the Au-particle, forming a NW, fig 2.2(c). To stop the growth, the supply of group III precursor is simply ended. To create NWs with complex structures one can either change the precursors, changing the material that will grow, fig 2.2(d), or increase the temperature to change the preferred [39] growth direction to introduce layer growth, i.e. growing walls on the NW to get core–shell structures, fig 2.2(e).

2.2 Nanowire doping

Over 20 years ago, K. Haraguchi et al. showed that it is possible to grow axial *p-n* junctions in NWs [40]. Since then large advances have been made in the field of NW growth and doping, but there are still many questions left to answer. Doping plays an important role in NW growth. The crystal structure has been shown to change when different dopants are introduced during NW growth [41]. It is also important to note that the carrier concentrations in NWs are not always proportional to doping concentrations. The control of the NW doping is of utmost importance for the operation characteristic of any NW device, and a lot of work has been put into the development of techniques to evaluate it.

Standard methods for doping planar devices are diffusion or ion implantation. To make axial doping profiles in NWs, these standard techniques are not ideal [42] since NWs typically are grown normal to the crystal surface. Instead, in-situ doping is used where the dopants are introduced during growth. As an effect, the doping profiles will be determined in large by the solubility of the dopants in the Au seed particle and their diffusion lengths. This can be used to create sharp doping profiles with interfaces which are only tens of nm wide [3].

The actual evaluation of the doping is also challenging since *standard* Hall measurements can not be used for NWs because of their small size (with specialized device fabrication for Hall measurements of NWs it has been shown that Hall measurements are possible for NWs [43]). Lately, a number of quantitative techniques have been explored by various groups. The most common of these is most probably the NW field-effect transistor (NW-FET) set-up. A NW is placed on an oxidized substrate and contacts are deposited to the ends of the NW. By changing the gate bias to the substrate and measuring the conductance

through the NW the carrier concentration and mobility of the carriers can be determined. This is however done using a series of assumptions [42]. Another major drawback of the NW-FET set-up is the contacting of the NW which is very challenging and requires oxide free NWs as well as high doping concentrations. It should also be noted that the NW-FET only gives information about the carrier concentration and mobility, which, for device optimization, is more important but it does not reveal the actual amount of dopants. Neither does it reveal the local distribution of the dopants over the length of a NW.

To evaluate the dopant concentration secondary-ion mass spectrometry or the more advanced technique, atom probe tomography (APT) can be used [44]. In APT a needle-shaped sample is needed, by pulsing the sample with an electric field and measuring the time-of-flight for the field emitted ions from the sample, a representation of the needle can be obtained with sub nm resolution. This method also has limitations. It is completely destructive since it has to remove an ion from the sample to detect it. The sample shape also puts limitations on what samples and sizes can be studied [45].

Another widely used method which in many respects is the opposite of APT is energy dispersive X-ray spectroscopy (EDX) where the resolution is more limited but the sample size- and structure constrictions are less confining, and it is also faster. EDX is an extension to a scanning- or tunneling electron microscope (SEM or TEM) with an extra detector that detects the photons with characteristic energy emitted from the various atoms in the sample.

2.3 Metal-semiconductor electrical contacts

The electrical contact between a semiconductor and a metal plays a crucial role in the performance of any semiconductor device [46]. A good contact is a contact which does not influence the performance of the device and has a small voltage drop over it compared to the rest of the device. These contacts are generally named ohmic contacts. Conversely, contacts which do affect the device performance are named rectifying contacts. In 1938, Schottky explained the rectifying behavior of these

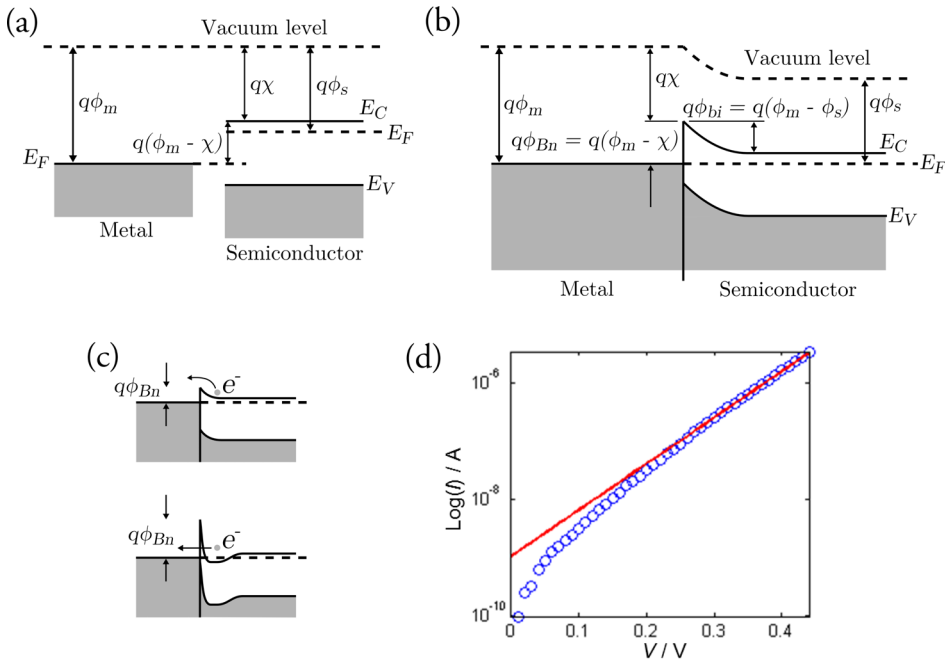

Figure 2.3: Energy band diagram of metal-semiconductor contacts and how to determine the Schottky barrier height. (a) The *n*-doped semiconductor and the metal in thermal nonequilibrium conditions. (b) The metal and semiconductor are now at thermal equilibrium and the barrier height ϕ_{Bn} and the built-in potential ϕ_{bi} are seen. (c) For an ohmic contact to be formed either a low ϕ_{Bn} (thermionic emission, top) and/or a high doping level closest to the metal (tunneling, bottom) is required. (d) Experimental current–voltage data (blue circles) from the Au-semiconductor interface of the NWs in Paper **V**. The red line is the simple linear regression used to determine I_S used to calculate ϕ_{Bn}.

contacts as a potential barrier arising from the space charges in the semiconductor [47]. This barrier now holds his name and it is known as the Schottky barrier.

To understand the nature of the different metal-semiconductor contacts, one starts with the ideal case of a metal brought into contact with a semiconductor, fig 2.3(a, b) [48]. In fig 2.3(a) the energy band diagrams are shown of a metal and an *n*-doped semiconductor isolated from each other. The work function of a material is defined as the energy difference between the Fermi level and the vacuum level. Typically the metal work function $q\phi_m$ and the semiconductor work function $q\phi_s$ are not the same. In fig 2.3(a) the electron affinity of the semiconductor $q\chi$ is also shown. It is the energy difference between the vacuum level and the conduction band of the semiconductor. With the two materials in contact, thermal equilibrium is established, and the Fermi levels of the two materials have to align. The vacuum level also has to be continuous which results

in the band-bending situation shown in fig 2.3(b). The potential barrier height the electrons in the metal have to overcome to enter the semiconductor is denoted $q\phi_{Bn}$ and it is the difference between $q\phi_m$ and $q\chi$:

$$q\phi_{Bn} = q\phi_m - q\chi. \quad (2.1)$$

Conversely, the barrier height the electrons in the semiconductor see is called the built-in potential $q\phi_{bi}$ and it is the difference between $q\phi_m$ and $q\phi_s$:

$$q\phi_{bi} = q\phi_m - q\phi_s. \quad (2.2)$$

The barrier height between a metal and a *p*-doped semiconductor is denoted $q\phi_{Bp}$ and it is given by

$$q\phi_{Bp} = E_g - (q\phi_m - q\chi), \quad (2.3)$$

where E_g is the band gap of the semiconductor.

The following text will be referring to *n*-doped semiconductors, but it is also valid for *p*-doped. To obtain an ohmic contact between a metal and a semiconductor a low barrier height ($q\phi_{Bn/p} \sim kT$) and/or high doping is demanded. With a low barrier height, there is no hindrance for thermionic emission of electrons between the semiconductor and the metal, fig 2.3(c) top. If $q\phi_{Bn/p} \gg kT$ a high doping concentration closest to the metal is required to shorten the depletion layer width sufficiently enough to allow for tunneling through the barrier, fig 2.3(c) bottom. If the barrier is too high and the doping is not high enough the contact will be rectifying, and the barrier will be referred to as a Schottky barrier.

At room temperature, the dominating transport mechanism over the Schottky barrier is thermionic emission of majority carriers from the semiconductor to the metal [48]. The current-voltage (*I-V*) behavior is

$$I = I_S\left(e^{\frac{qV}{kT}} - 1\right), \quad (2.4)$$

$$I_S = AA^*T^2e^{-\frac{q\phi_{Bn}}{kT}}, \quad (2.5)$$

where I_S is the saturation current, A the interface area of the contact, A^* the effective Richardson constant which is dependent on the semiconductor material, and T is the absolute temperature. For $qV \gg kT$ the *I–V* behavior, equation 2.4, can be rewritten as

$$\log(I) = V\frac{q}{\eta kT}\log(e) + \log(I_S), \quad (2.6)$$

where the ideality factor η is added to account for different types of currents. An ideality factor of 1 means that the ideal diffusion current completely dominates, whereas an ideality factor of 2 indicates that recombination currents are dominating. By plotting experimental *I*–*V* values, fig 2.3(d), and making a simple linear regression for values $V \gg kT/q$, the value for I_S can be determined at $V = 0$ for the simple linear regression, assuming diffusion currents to be dominating. The value for I_S is then used to determine the Schottky barrier height by writing equation 2.5 as

$$\phi_{Bn} = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_S}\right). \quad (2.7)$$

This method was used for determining the Schottky barrier at the Au-semiconductor interface of the NWs in Paper **V**.

Equation 2.1 is only true for the ideal case, and for real world metal-semiconductor contacts more factors contribute to an eventual Schottky barrier height. The termination of the semiconductor crystal at the metal interface induces surface states which may very well be situated in the band gap and influence the barrier height [49]. The structure and dimensions of the metal-semiconductor contacts can also influence the height [50]. In Paper **V** we also discuss the formation of a dipole layer between the metal and semiconductor which can reduce the height. The semiconductor, in this case, is GaAs NWs grown in the (111)B plane with the top Au-seed-particle acting as the metal. The interface between the NWs and the Au consists of only As atoms due to the orientation the NW growth. The As atoms in contact with the Au atoms have a lower electronegativity compared to their neighboring Ga atoms resulting in a dipole layer which in turn lowers the Schottky barrier.

2.4 Devices

The most basic NW device is simply contacted NWs. LEDs, solar cells, and transistors can all be made by using NWs still standing on their growth substrate, as-grown [51-53]. The growth substrate then acts as one contact to the NWs and another contact is deposited on top of the NW array. For the transistors, a third contact is needed for the gate. This set-up, with the NWs as-grown, is ideal for industry applications because of the relative few process steps needed to create the devices. In Paper **I** and **II**, however, another device design is used to study the NWs, namely the before mentioned FET set-up. This design is used purely for research purposes to enable investigation of the NW properties.

Constructing devices out of NWs has been shown to improve device performances compared to bulk devices. This can be measured as better energy conversion efficiency for solar cells or luminous efficacy for LEDs. These properties are straightforward to measure but, they will only tell you whether your device is working well or not, not how, and maybe even more important, why. To investigate how and why various NW devices work as they do, we have set out to develop novel techniques as well as combining existing methods to investigate the properties of NW devices. Our findings are presented in Papers **I–VII** in the second part of this thesis.

Moore's law states that the number of transistors on integrated circuits will double approximately every two years [54]. However, Moore's law is not a law but rather a prediction and it has been fulfilled (with slight modifications) during the last decades by the downscaling of the planar MOSFET. This is because the semiconductor industry adopted the statement and has used it as the road map for their development. By making the transistors smaller, not only has the performance improved but the level of integration has increased drastically and the power consumption per function implemented has gone down [55]. The downscaling can not continue ad infinitum due to quantum effects and problems with power dissipation (and in turn overheating), so researchers are now developing new ideas and techniques to continue Moore's law. The NW wrap gate MOSFET has a gate that encloses the transistor channel as compared to standard planar MOSFET where the gate sits on top, enabling improved electrostatic control within the channel [56]. This makes further scaling of the gate possible, or one does not have to scale the oxide as much. With sub 5 nm NW diameter the device can work in the quantum capacitance regime with lower power consumption as a result as well [55, 57]. Utilizing other gate oxides with higher relative dielectric constant also help improve the performance of the MOSFET. In Papers **VI** and **VII**, the properties of one such oxide, HfO_2, and the mechanisms behind its growth are investigated.

2.5 Atomic layer deposition & high-k dielectrics

In the semiconductor industry, Si has been the material of choice in large part due to its native oxide, SiO_2, which easily forms. The oxide plays a crucial part in all transistors as it forms the insulating layer between the gate and the channel. The effectiveness of the gate to introduce charge carriers in the channel is directly proportional to the capacitance of the oxide. The drain current is proportional to the number of charge carriers in the channel, and it is one of the key output parameters of the transistor. Downscaling has been the driving force behind the

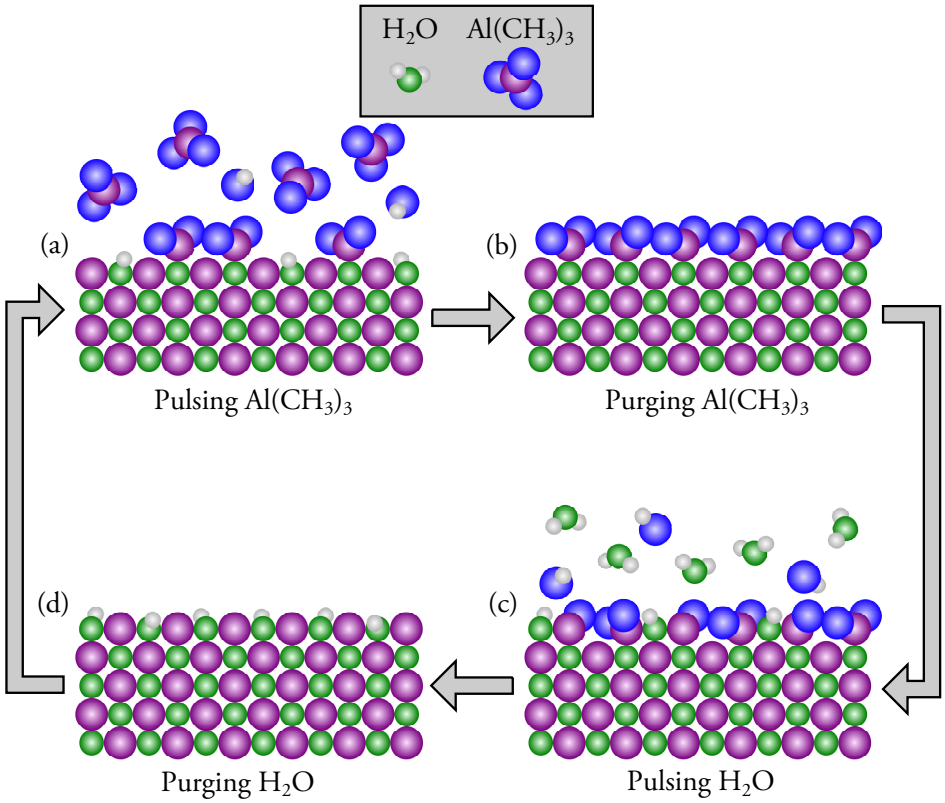

Figure 2.4: Schematic presentation of the ALD process, in this case for the forming of Al_2O_3. In step (a) the precursor $Al(CH_3)_3$ is dosed over an already formed Al_2O_3 layer (which is terminated with O-H groups) and an atomic layer of $Al(CH_3)_2$ is formed covering the oxide. During this process, excess CH_4 (gas) is formed. In step (b) the sample is purged, and all that is remaining is the $Al(CH_3)_2$ layer. In step (c) the sample is dosed with H_2O and a new Al_2O_3 layer (terminated with O-H groups) is formed. Also in this process excess CH_4 (gas) is formed. In step (d) the sample is once again purged and the cycle can start over.

increase in processor speeds but the limit when the electrons start to tunnel through the gate oxide (approx. 2 nm oxide thickness), creating leakage currents and thereby increased power consumption, has been reached.

The capacitance, C, of the MOSFET oxide can be modeled as a parallel plate capacitor,

$$C = \frac{\kappa \epsilon_0 A}{t}, \quad (2.8)$$

where A is the area of the oxide, t is the thickness, ϵ_0 is the vacuum permittivity, and κ is the relative dielectric constant. Given a certain dimension of our

transistor, A will be given, and t can not be smaller than 2 nm. That leaves κ as the only parameter left to alter to increase the capacitance. Materials with a high κ are often referred to as "high-κ" or simply "high-k" dielectrics. Typical high-k dielectric materials include Al_2O_3 and HfO_2. In Papers **VI** and **VII**, we study the structure of HfO_2 grown with ALD and also the actual ALD growth process of HfO_2.

When it comes to deposition of these high-k materials, as thin conformal films, on high aspect structures, such as standing NWs, atomic layer deposition (ALD) is considered one of the most promising techniques [58]. ALD was invented by Tuomo Suntola in 1974 but was then called atomic layer epitaxy (ALE). However, most films grown are not epitaxially grown on the underlying substrate and often films grown are amorphous. Hence the more accurate description atomic layer *deposition* has been adopted. ALD is a sequential, self-limiting surface reaction technique and can be described as consisting of four essential steps [59], fig 2.4(a-d): 1) first precursor exposure, 2) purging of said precursor and byproducts, 3) second precursor exposure, and 4) purging of the second precursor and byproducts. This process is then iterated until the desired number of atomic layers have been grown. The main and distinctive difference between ALD and MOVPE is that ALD is self-limiting; the precursors will not bind to themselves, allowing the ALD film to grow one mono layer per iteration. In MOVPE, due to variations over a sample in precursor flux, adsorption probabilities, and surface diffusion, growth speeds will vary across the sample. This causes nonconformal growth in MOVPE where different precursors are present at the same time. But due to the self-limiting properties due to the sequential dosing of the precursors in ALD, conformal growth can be achieved even on high aspect ratio structures. The self-limiting properties also ensure atomic monolayer precision even when growing nm thick layers.

2.6 Nanowire cleaning

All NWs studied during the work for this thesis have been grown by collaborating groups. The transfer of NWs from MOVPE chambers to our various experimental set-ups is done in air under atmospheric pressure. The use of vacuum suite cases where the NWs are kept at low pressures under all times could, in theory, be implemented. At the time of writing this thesis, though, our equipment does not have the specific adaptations to support such an elaborate transfer system. III-V semiconductor materials will oxidize under atmospheric pressures in air, forming a native oxide of 1-2 nm thickness at the surface. This oxide formation is detrimental for device performances, and it is circumvented by encapsulating

processed devices in buffer materials. This procedure will, however, make surface studies of the NWs impossible. Without the encapsulation the oxide will however also greatly reduce the effectiveness of many surface science techniques since the surface of interest will be buried underneath; in XPS the signal from the III-V semiconductor will be greatly reduced and for STM the oxide might even cause the tip to crash.

An oxide removal technique which has been used extensively for metal crystals is Ar-ion sputtering [60]. To ensure high surface crystal quality, the sample has to be annealed afterward to remove trapped Ar atoms and to reduce induced surface roughness. However for III-V semiconductors Ar-ion sputtering induces amorphous layers as well as defects which are hard to anneal away [60]. This is especially true for III-V NWs which in many cases will be destroyed if treated with the temperatures needed to anneal away defects.

Instead, atomic hydrogen cleaning (AHC) has been shown to successfully remove surface contaminants on III-V semiconductor surfaces, especially oxygen and carbon [61]. AHC can be performed inside the preparation chamber of the STM under UHV condition. The sample is annealed (for InAs typically to 650 K) under a flux of atomic hydrogen radicals (H*) which are formed with a thermal cracker (typically at 2000 K) attached to the preparation chamber. The H* react with the surface oxides, hydrocarbons, and other surface contaminants and the products are desorbed leaving behind a clean III-V semiconductor surface. The H* have very low kinetic energies (typically less than 1 eV) limiting their interaction with the III-V semiconductor surface to the top atomic layers. This greatly limits their incorporation in the III-V semiconductor [62]. This method is instrumental for much of the STM work on NWs at our division [63-65], and in Paper **I** this method is used to enable STM investigations of NW side facets.

Thermal cleaning of III-V semiconductors without H* is also possible, but it requires higher temperatures which create a problem due to the congruent evaporation temperatures (T_C) of III-V semiconductors. At temperatures above T_C, the rate of evaporation of the group V material will be larger than for the group III leading to a change in the surface chemical composition.

Cleaning NWs is paramount when studying their facets, but it can also be used as a tool to study how surface states on the NW affect the NW devices performance. In Paper **III** we present supporting information on how the performance of *p-i-n* (*p*-doped, intrinsically doped, *n*-doped) junction InP NWs is greatly improved upon removal of the surface oxides with AHC. In Paper **IV** we see how the surface states of InAs NWs affect the NW conductance differently depending on the crystal structure of the NWs.

3 Experimental techniques

In this chapter, the two main experimental techniques relevant for this work, will be described, as well as the new methods developed for these. The two main techniques are scanning tunneling microscopy (STM) and X-ray photoelectron spectroscopy (XPS). The new methods are scanning probe microscopy (SPM) on NW devices, STM in top contact mode, hard X-ray photoelectron spectroscopy (HAXPES), and ambient pressure XPS. Both main techniques are usually referred to as surface sensitive techniques, but there are many ways to define what surface sensitive means. When using surface science techniques, one has to be aware of the penetration depth of said technique. The technique might show information of the top most layer of atoms or from tens of nm under the surface. STM and XPS are on either side of the surface sensitive–spectrum. STM probes the outermost atomic layer structure and its electronic properties, and XPS give information about the elemental composition of materials from up to 20 nm below the surface. Most surface science techniques require ultra-high vacuum (UHV) conditions, pressure below 10^{-9} mbar, to work. There are two main reasons for this. First is the contamination of the sample surface due to impingement of the atoms/molecules in the surrounding atmosphere on the surface, which is directly proportional to the surrounding pressure. At room temperature, and pressures of 10^{-6} mbar, a surface with a sticking coefficient of 1 (typical metal) will be covered in a layer of atoms in roughly one second. The second reason for using UHV conditions is the detection of the kinetic energy of electrons used in many techniques. An electron emitted from a solid into a gas will travel a certain distance before inelastically colliding with the atoms/molecules in the gas, losing kinetic energy. This process, known as inelastic scattering, is reversely proportional to the gas pressure. Once an electron has lost kinetic energy, it is no longer interesting to detect and it will only contribute to the background noise.

3.1 Scanning tunneling microscopy

The STM is a surface sensitive technique which utilizes the quantum mechanical tunneling of electrons to image surfaces at the atomic level. In 1986, Dr. Gerd

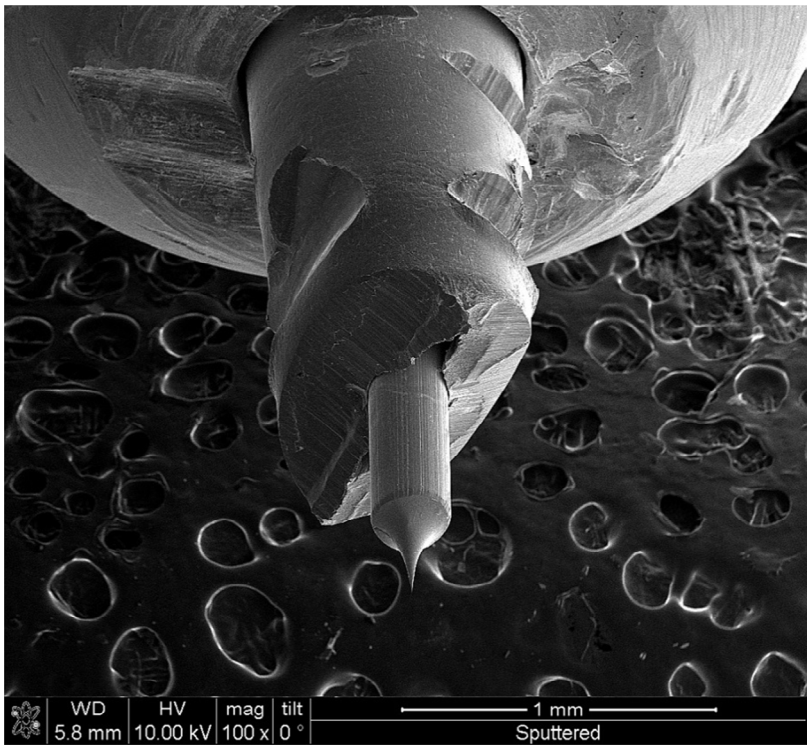

Figure 3.1: A low magnification scanning electron micrograph of an STM tip made from an etched W wire. The black background with holes is the carbon tape with which the tip is mounted in the scanning electron microscope. The etched W tip itself is clamped in a steel tube which in turn is mounted in the tip-holder. The indentations on the steel tube are from the pliers used when fixating the tip.

Binnig and Dr. Heinrich Rohrer at the IBM Research Laboratory in Zurich, Switzerland, were awarded the Nobel Prize in physics for their design of the STM which they reported on five years earlier [66]. This revolutionizing tool enables resolution of individual atoms and localized electronic states on the surface of any conducting or semiconducting material. In Papers **I-V** we utilize this tool to investigate NWs in both conventional and unconventional ways.

The name of the technique arises from the fact that an atomically sharp probe is raster *scanned* over a surface while a *tunneling* current between the probe and the surface is measured. The probe and the surface are never in contact during normal STM investigations. The signal recorded – either the strength of the tunneling current or the height of the tip – is made into an image showing the properties of the studied surface. The probe used is usually an electrochemically etched W wire, fig 3.1, or a cut Pt/Ir wire which forms an atomically sharp tip. The surface is the surface of either a metal or a semiconducting material. The spatial resolution is

around 0.1 nm in plane with the surface studied and 10 pm normal to the surface plane. The image repetition rate is in the order of minutes per image but can, under the right circumstances be as high as 25 images per second [67].

The current measured cannot be explained with classical physics since the work function (the energy needed to bring an electron from the Fermi level into vacuum) for an electron in a solid is typically in the eV range while the thermal energy available at room temperature to overcome this barrier is only 25 meV. Instead, a quantum mechanic approach is needed to explain the flow of electrons between the tip and the sample. In quantum theory, and then also reality, an electron has a certain probability to be anywhere in space at a certain time (granted, the probability will be infinitesimally small everywhere except for within a small volume in space) [68]. This probability cloud can then extend from the outmost point of the tip, through the distance between tip and sample, and into the sample. If there is an electronic state in the sample that the electron can occupy then the electron in the tip has a certain probability to occupy that state. If it does so, it has tunneled from the tip to the sample and thus created a tunneling current.

3.1.1 Electron tunneling

Tunneling between two conducting materials may occur when they are so close together that the electron wave functions at the Fermi level of each material overlap significantly due to leak out from the electrons potential confinement wells. This leak out has a typical inverse decay length, K, which can be described as

$$K = \hbar^{-1}(2m\phi)^{\frac{1}{2}}, \quad (3.1)$$

where m is the electronic mass and ϕ is the effective local work function. This can be rewritten as $K \approx 0.51\phi^{1/2}$ where K is measured in Å^{-1} (1 Å = 0.1 nm) and ϕ in eV. By bringing the tip and the sample close enough together (< 1 nm) and applying a potential difference between the same, a tunneling current, I_T, will arise which relates to the tip-sample distance, d, as (fig 3.2(a))

$$I_T \propto e^{-2Kd}. \quad (3.2)$$

It is important to note that d is actually the distance between the two electronic states which the electron tunnels between. Imaging larger objects (at the nm range) with an STM will reveal the structure morphology but when imaging individual atoms the spatial structure of the electronic states of both the tip and

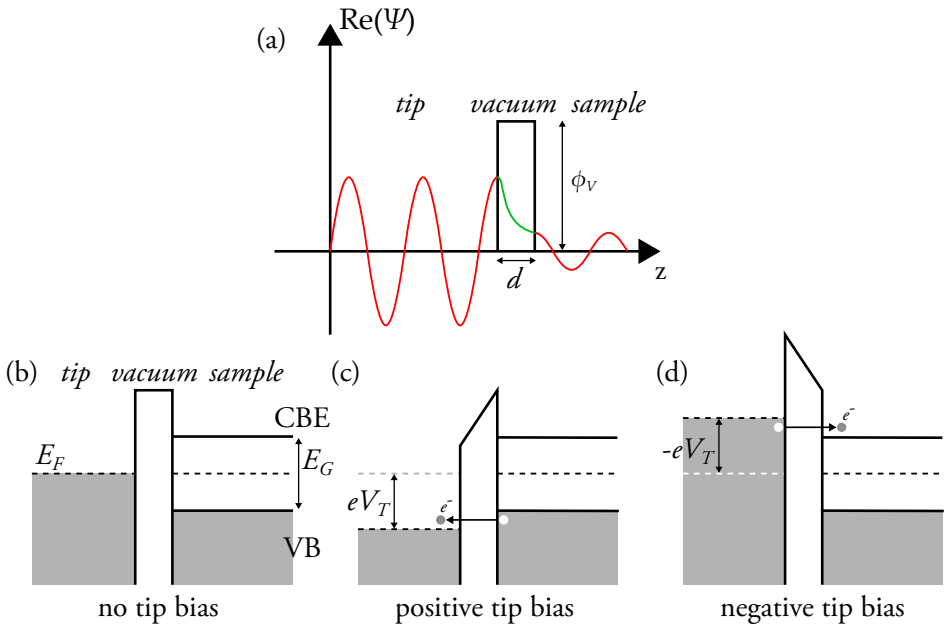

Figure 3.2: (a) The wave function of an electron as it tunnels from the tip into the sample (assuming that the tip and sample have the same work function). The potential barrier is the vacuum between the tip and the sample with thickness d and potential height ϕ_V. (b) Band diagram of the tip and sample with no applied bias and hence no tunneling. (c) The band diagram with positive tip bias (V_T), showing the electrons tunneling from the valence band (VB) of the semiconductor, through the vacuum to the empty states in the tip. (d) With negative tip bias ($-V_T$) the electrons in the tip can tunnel to the empty states in the conduction band instead. Only the conduction band edge (CBE) is shown in (b-d)

the atoms will influence the resulting image and make interpretation much less straight forward. For a typical work function of 4 eV ($K \approx 1$ Å), the tunneling current will change with almost an order of magnitude if the tip-sample distance changes by 1 Å. This is the fundamental physics behind the good spatial resolution of an STM. If the tunneling current can be kept constant to within a few percent, the tip–sample distance will only vary with roughly 0.01 Å.

3.1.2 Tunneling current

The probability, T, for an electron to tunnel from an initial state with energy E_i through a potential barrier to a final state with energy E_f is stated by Fermi's golden rule to be

$$T = \frac{2\pi}{\hbar}\left|M_{i,f}\right|^2 \delta(E_i - E_f), \qquad (3.3)$$

where $M_{i,f}$ is the tunneling matrix element between the initial and final state. The δ-function merely states that there only is a tunneling probability between states of the same energy. By using first-order perturbation theory, the tunneling current, I_T, between two states can then be described as

$$I_T = \frac{2\pi e}{\hbar}\sum_{i,f} f(E_i)[1 - f(E_f + eV)]\left|M_{i,f}\right|^2 \delta(E_i - E_f), \quad (3.4)$$

where $f(E)$ is the Fermi-Dirac distribution function and V is the applied voltage. The tunneling matrix can, according to Bardeen, be expressed as

$$M_{i,f} = -\frac{\hbar}{2m}\int(\psi_i^* \nabla\psi_f - \psi_i \nabla\psi_f^*)dS, \quad (3.5)$$

where $\psi_{i,f}$ are the wave functions of the states, ψ^* is the complex conjugate, and the integral is taken over a surface lying between the initial and final state, i.e. in the potential barrier [69]. To calculate the tunneling current one thus has to know the wave functions of the initial and final state which is far from trivial. By making the assumptions that: the apex of the tip has an asymptotic spherical form, the initial and final states are s-wave functions, and the temperature is low, Tersoff and Hamann [70] managed, in 1985, to describe the tunneling current between the tip and the sample for an STM as

$$I_T \propto \rho_t \int_0^{eV_T} \rho_{s,loc}(\overrightarrow{r_0}, E_F + \varepsilon)d\varepsilon, \quad (3.6)$$

where ρ_t is the local density of states (LDOS) for the apex atom of the tip and $\rho_{s,loc}(r,E)$ is the LDOS at the surface at position r and energy E. The formula tells us that the tunneling current is proportional to the integrated LDOS of the sample from the Fermi level E_F to $E_F + eV_T$, fig 3.2(c, d).

3.1.3 STM operation

There are two standard working principles to run an STM: constant current mode and constant height mode. In both modes, a potential difference is applied between the tip and sample and the tunneling current, which is exponentially proportional to the tip–sample distance, is measured.

In constant current mode, the tunneling current is kept constant, while the tip is scanned over the surface, by using an electronic feedback loop which continuously changes the height of the tip. The tip height is controlled by varying the potential applied to a piezoceramic actuator on which the tip is mounted, fig 3.3.

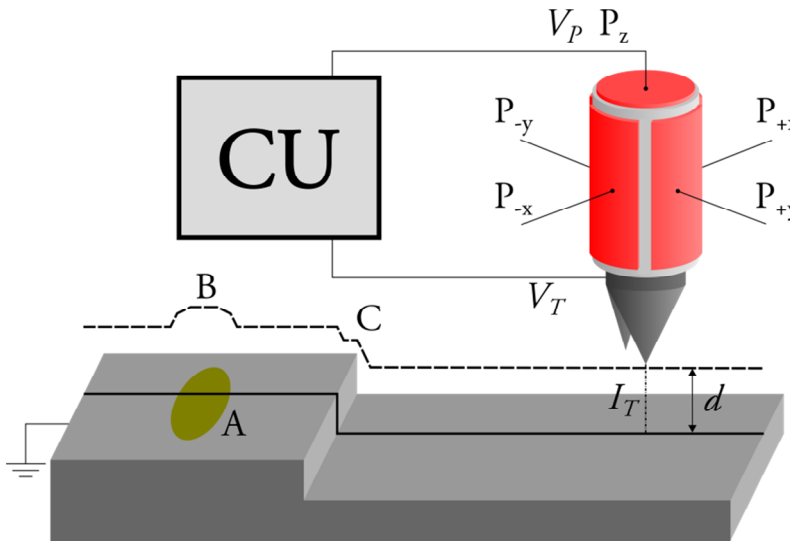

Figure 3.3: A schematic representation of an STM, the size of the objects are not to scale. The piezo contacts (P) change the shape of the piezoceramic tube, the scanning motion is governed by the x and y contacts P_x and P_y. The controller unit (CU) keeps the tunneling current I_T constant by varying the bias V_P to the z contact P_z and records the height of the tip (dashed line). Irregularities in the work function (A) of the surface will give rise to variations in the tip height (B). The shape of the tip will also influence the recorded topography (C).

A piezoceramic is a material, e.g. lead zirconate titanate, which can translate an electric field to mechanical strain.

In constant height mode, the tip height is kept constant, and the varying tunneling current is measured instead. Constant height mode is a faster imaging technique, but the drawback is that the sample roughness tolerance is very limited due to the very short tip-sample distances (~10Å) used when performing STM.

All standard STM work performed by me during the timespan of this thesis has been conducted using constant current mode. The resulting images will then show the recorded tip height, fig 3.3(dashed line), at each point in a predefined matrix. However, it is important to remember that the height of the tip (i.e. the brightness in the STM image) is not only dependent of the sample corrugation but also the electronic structure of the sample, fig 3.3(A). Since a change in the density of the electronic states at the surface will change the amount of possible states for the electrons to tunnel between, the tip–sample distance will have to accommodate to keep the set tunnel bias, fig 3.3(B). This leads to features in STM images where brighter areas might not be higher areas but rather areas where the density of electronic states is larger, and vice versa for darker areas. The shape of the tip also factors in in the quality of the image recorded. A common, and unwanted, feature

is the double tip, or even multi tip. If the tip is not a perfect tip, it might have more than one feature which can induce tunneling depending on the surface structure. The double tip feature is often seen as e.g. a step edge having an extra step, fig 3.3(C).

The three main input parameters the operator of an STM, in constant current mode, varies to obtain a good quality image are: 1) The potential applied between tip and sample, V_T, determines which states the electrons can tunnel from between the tip and the sample, typically between -3 and 3 V. The resulting current obtained when applying V_T will be a sum of the electrons tunneling from all the states between the Fermi level and $E_F + eV_T$. 2) The tunneling current (typically between 10 and 300 pA) sets the desired value for the feedback loop and thus the tip–sample distance. 3) The loop gain of the feedback (typically between 0.1 and 2 %) determines how fast the STM responds to changes in sample height; too high gain creates instability though.

3.1.4 qPlus mode

One major drawback of the STM is the inability to scan on nonconducting materials. This lack of ability is especially limiting if one wants to investigate NW devices made on nonconducting substrates. NW devices studied in Paper **I** and **II** are of the NW-FET design mentioned in chapter 2.2 where III-V semiconductor NWs are deposited on an oxidized Si substrate, and metallic contacts are deposited contacting the ends of the NW, fig 3.4(a, c). If one is to investigate these samples with an STM, extreme care will have to be put into not scanning on the SiO_2 which will inevitably deteriorate the tip. In practice, the method is too time–consuming, but an alternative method in the combined STM/AFM is available. AFM stands for atomic force microscopy and is similar to STM with respect to the experimental set-up, but the physical interaction between the tip and sample is fundamentally different. The tunneling tip of the STM is replaced by a force sensor in the AFM. If the force sensor is conducting an instrument which can do both STM and AFM simultaneously can be realized, the STM/AFM, fig 3.4(b). This instrument has been used to locate NWs (in AFM mode) on the SiO_2, once located the NWs can then be investigated with the STM.

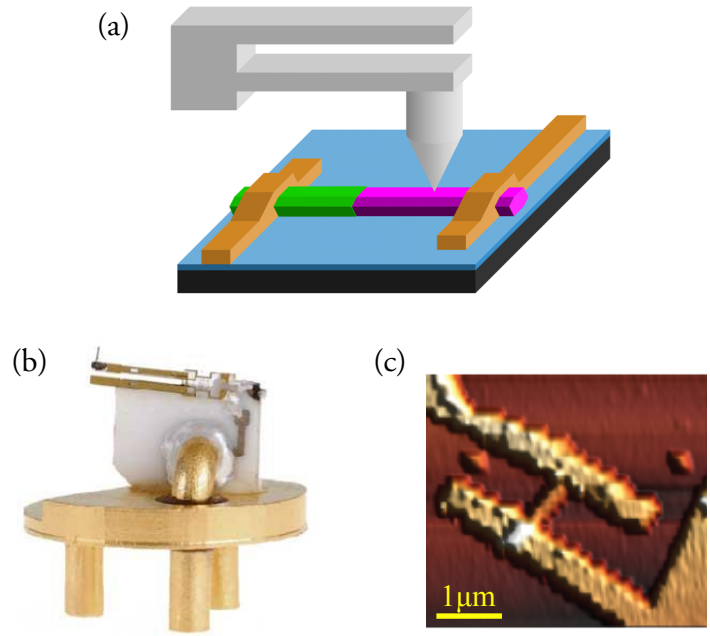

Figure 3.4: (a) Schematic representation of the NW-FET sample with the NW, the metal contacts, the qPlus tip and tuning fork, and the large nonconducting SiO_2 areas which are not accessible in STM mode. (b) The STM/AFM tip mounted on a quartz tuning fork (qPlus) which in turn is secured to the tip holder [71]. (c) Low resolution AFM image overview of a NW-FET device with the NW in the middle of the image contacted with metallic contacts.

The major advantage of AFM compared to STM is the ability to scan on any type of surface. The drawbacks of AFM compared to the STM, for our measurements, are however quite a few. The advantages of the standard STM are:

- The strong tunneling current dependence on tip-sample distance of the STM enables atomic resolution even with relatively blunt tips since there always will be one atom protruding from the tip that carries most of the tunneling.
- The tunneling current can be measured in nA allowing for very good signal-to-noise ratio.
- The tunneling current is a monotonic function of the tip-sample distance which makes it easy to maintain a stable feedback loop.
- Scanning tunneling spectroscopy (STS) is possible (see chapter 3.2).

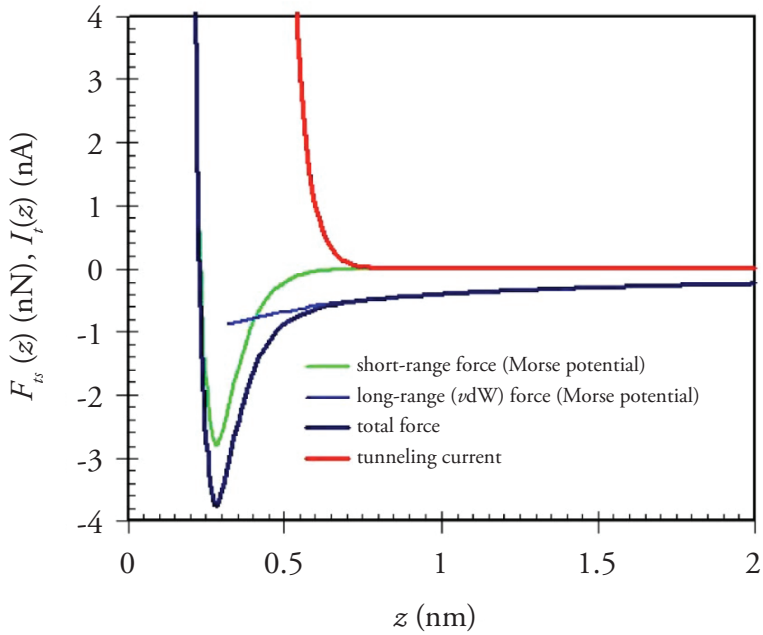

Figure 3.5: Graph showing the tunneling current I_t (red) and force F_{ts} (black) as a function of the distance z defined as the distance between the center of the outermost tip atom and the plane defined by the centers of the surface atoms. Image adopted from ref. [72].

None of these conditions are met for the AFM making it a more complex technique to develop and master. In all AFMs, the force sensor is a tip which is mounted on a cantilever. Bringing the AFM tip close to the sample surface will create a force acting on the tip, fig 3.5, thus affecting the cantilever. This force, or some entity derived from it, will be used for all operation modes of AFM as the image signal. The force has many sources of origin. In vacuum, the chemical forces are acting on the short range (sub–nm), but there are also electrostatic, van der Waals, and magnetic forces acting on a longer range (up to 100 nm) [72]. These forces combined create the non-monotonic dependence of the force as a function of the tip–sample distance.

In the first AFM the force acting on the tip was actually measured with an STM, as a deflection of the cantilever [73]. Later designs used optical as well as electrical methods to determine the cantilever deflection [74]. The AFM mode used during the timespan of this thesis (dynamic operation frequency-modulated, or short FM) however does not rely on the deflection of the cantilever per se, but rather the change in frequency of the cantilever. In dynamic operation mode, the cantilever is mounted on an actuator which excites an oscillation of the cantilever. The

cantilever itself is a quarts tuning fork where one prong is fixed to the tip holder, fig 3.4(b), called a qPlus sensor. The frequency of the cantilever is measured by monitoring the electric charge build-up caused by the piezoelectric effect as the prong vibrates. In FM-AFM the oscillation is kept at a constant amplitude and the forces between the tip and sample will influence the frequency f of the cantilever as $f = f_0 + \Delta f$, where f_0 is the cantilever eigenfrequency and Δf is the shift given by

$$\Delta f = \frac{k_{ts}}{2k} f_0, \quad (3.7)$$

where k_{ts} is the tip–sample potential and k is the spring constant of the cantilever. The frequency shift will then give the force gradient which can be used as the image signal.

3.2 Scanning tunneling spectroscopy

The tunneling current recorded when performing STM is proportional to the integrated LDOS of the sample from the Fermi level E_F to $E_F + eV_T$, where V_T is the tip bias. This is utilized in scanning tunneling spectroscopy (STS) where the LDOS of the sample surface can be determined. For semiconductor materials, the LDOS will give information about the band gap of the material as well as if there are any states within the bandgap. STS and STM are typically performed in conjunction with each other; the STM is used to map an area and then the tip is moved to a place of interest and a point spectrum is recorded, STS. When recording a spectrum the raster motion of the tip is disabled as well as the feedback loop, the tip bias V_T is then swept and the tunneling current I_T is measured as a function of the bias, creating an *I-V* spectrum, fig 3.6. Since the feedback loop is disconnected, the tip–sample distance may vary during spectrum recording due to vibrations, thermal drift, and/or creep in the piezo crystals. These unwanted distance variations have to be kept as small as possible since they will not only deteriorate the spectrum but might also damage the tip.

In order to obtain the sample surface LDOS from the STS data, the differential conductance as a function of applied bias (dI/dV - V) is needed. This can be achieved by either numerically differentiating the measured *I-V* spectrum or by directly measuring the differential conductance. The numerical method is easier from an experimental point of view, but it also amplifies any noise found in the *I-V* measurements. A better approach is the direct measurement which is achieved by applying a low amplitude, high-frequency sinusoidal voltage on top of the tip bias. Using a lock-in amplifier, the resulting alternating current can be detected, which in turn, together with the bias modulation, will give the differential conductance.

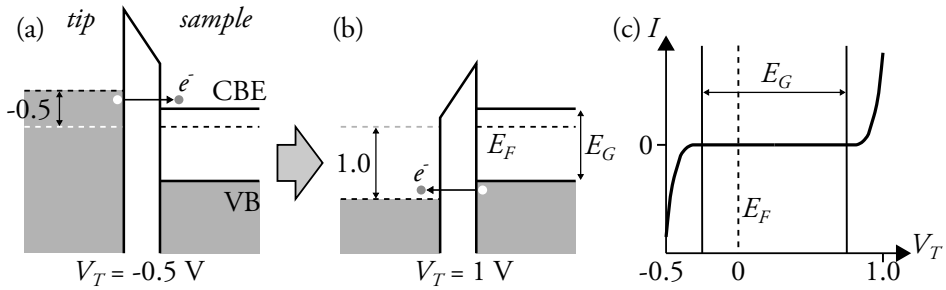

Figure 3.6: Schematic representation of STS. (a) Band diagram of a *n*-doped semiconductor when applying - 0.5 V tip bias, V_T. The tip bias is then ramped to 1 V (b) and the resulting *I-V* curve (c) will show the general features of the sample bandstructure. When V_T is within the band gap, no tunneling will occur since there are no states in the band gap (c). The doping of the sample will also be visible as a shift of the Fermi level E_F (which is always at V_T = 0 V) from the mid gap position in the band gap E_G.

3.2.1 Variable z-mode and normalized spectra

When recording *I-V* spectra with STS, the current is limited to a couple of orders of magnitude; too large current will damage either tip or sample, and too low current can not simply be resolved. This is especially true for semiconductors with considerable band gaps. To determine the band gap onsets and also resolve potential states within the band gap, the variable z-mode is utilized. This mode was presented by Mårtensson and Feenstra [75] in 1989. In variable z-mode, the spectroscopy is performed just as in ordinary STS, but in addition, the tip–sample distance *d* is changed as

$$d(V) = d_0 + a|V_T| \quad (3.8)$$

where V_T is the applied bias, *a* is a parameter chosen by the operator, and d_0 will be the distance at V_T = 0, fig 3.7(a). A typical value for *a* is in the range of 1 Å/V_T. The tunneling current is exponentially dependent on the tip-sample distance which means that the varied z-mode will increase the tunneling current at V_T close to zero, increasing the current resolution for low voltages. The current resolution can be increased by more than two orders of magnitude compared to STS without variable z-mode [76].

In variable z-mode the d*I*/d*V* signal (differential conductance) is a function of tip–sample distance as well as V_T, but Feenstra et al. showed that by normalizing to the total conductance (*I*/*V*) the tip–sample distance dependence cancels out [77]. This approach works well

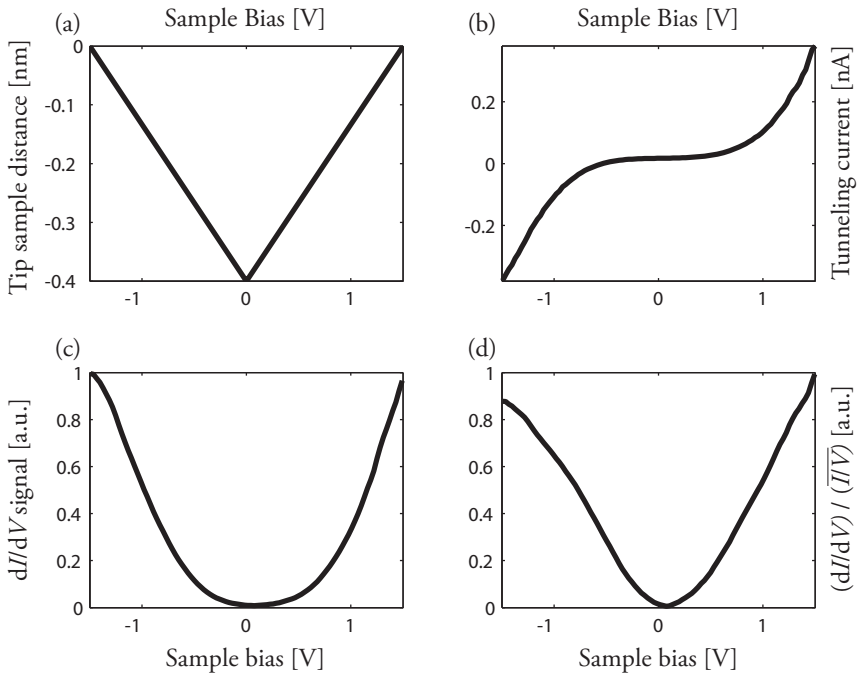

Figure 3.7: STS data acquired from a biased InAs/GaSb NW at the GaSb part. 250 spectra were recorded in a predefined matrix, (b-d) show one of these. (a) The tip-sample distance as a function of the sample bias with respect to starting tip-sample distance at -1.5 V. (b) The recorded *I-V* spectrum. (c) The d*I*/d*V* signal measured at the same time as in (b) by the lock-in amplifier. (d) The final spectrum where the d*I*/d*V* has been broadened by the normalized *I*/*V* spectra.

for metals but semiconductors with their band gap introduce a new problem. When performing STS on semiconductors, the current approaches zero faster than the conductivity which leads to errors in the normalizing procedure especially at the band gap, the most interesting area. By broadening the total conductance, the divergence can be avoided. The broadening can be done in several ways, the easiest being to simply add a small constant value. All spectra analyzed during the time span of this thesis have been broadened using a convolution between the total conductance and an exponential function as described in [76] as:

$$\overline{I/V} = \int_{-\infty}^{\infty} (I(V')/V') exp\left\{\frac{-|V'-V|}{\Delta V}\right\} dV' \qquad (3.9)$$

The broadened total conductance is convoluted over an infinite voltage integral at every V' and weighted by an exponential function with the width ΔV. When utilizing this convolution for measured spectra one has to redefine the integral as a summation and also find more suitable limits for the summation. By extending

the measured I/V by ΔV on either side and defining the limits as the first and last data point, the broadening can be carried out using a computer. ΔV should be chosen to be at least half the band gap energy to avoid any divergence. In fig 3.7(d) the differential conductance normalized with the broadened total conductance using this technique is shown. Here a ΔV of 0.5 V was used.

3.3 Scanning probe microscopy on NW devices

STM is a surface science technique developed to investigate flat, conductive surfaces at the atomic scale. To scan on samples with deposited NWs lying down on the surface, creating obstacles of several hundreds of nm in height, would be considered challenging by many STM users. To find a NW and subsequently scan on top of the NW side facets with atomic resolution, special considerations have to be made. These include low tunneling current (to create large tip–sample separation), fast feedback, slow scan speed, and large z-piezo range to avoid crashing into, or moving, the NWs. This technique has been developed at our division, and it has been used to characterize the atomic structure of NW side facets, the electronic properties of NWs, doping profiles, and for determination of band gap structure [63-65, 78, 79]. A further development of this technique is to perform STM on NW devices where this information obtained for the NW can directly be coupled to the specific NW device characteristics. The differences, compared to performing STM on free-lying NWs, are that the sample preparation is more complicated, one has to find a specific NW, and the NWs are typically deposited on an insulating substrate.

In Paper **I** STM measurements on NW-FET devices were conducted which meant that special considerations had to be made because of the insulating surfaces, high aspect ratio geometries, and the relatively large scales present. Here NWs consisting of one InAs- and one GaSb segment were deposited on an oxidized Si substrate, and Ti/Au leads and guiding patterns were defined using electron beam lithography. The leads (golden features in fig 3.8(a)) were connected to either end of a NW and could be biased using an external power supply. This meant that the NW, once located, could be studied with STM while varying the potential along the NW (during operation). The wires attached to the Au pads in fig 3.8(a) are Pt wires used to create contact between the Ti/Au leads on the sample and the sample plate on which the sample is mounted. The sample plate is in turn connected to the external power supply which allows for the biasing of the NWs.

To perform these experiments, the before mentioned considerations mean that, certain preparations and a specific procedure needed to be developed. Firstly, oxides and other contaminating species have to be removed from the surfaces of the NWs. This procedure is thoroughly described in chapter 2.6 for free laying NWs. The next step is to use the before mentioned combined STM/AFM to enable scanning on the whole sample without deteriorating the tip. Here it might be prudent to point out that the STM/AFM uses the same tip when performing both STM and AFM. While scanning in AFM mode, the specific NW which is

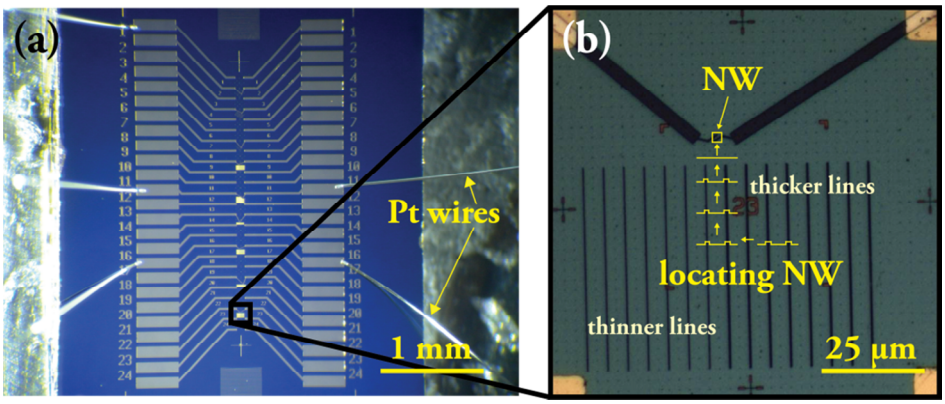

Figure 3.8: The sample design used for the experiments in Papers **I** and **II**. (a) Optical image showing the Ti/Au leads going to specific NWs at the center of the sample where six of the guiding pattern areas are visible. The Pt wires connecting the sample to the sample plate are also visible. (b) Optical micrograph of the lead ends (thicker black lines) and the guiding pattern used to locate the specific NW (black verticle lines at the bottom). Here also the basic principle used to locate NWs is depicted. By recording single line scans on the guiding pattern, one can relatively easy find the position of the NW because the lines in the guiding pattern have different width depending on which side of the NW they are.

externally contacted can be located. The process of finding a specific NW is not straight forward due to two factors.

The first factor is the initial positioning of the tip which is performed using an optical camera with 30 times magnification. It is possible, under the best of circumstances, when the lighting of the tip and the sample is just right, to position the tip somewhere roughly within a 100x100 μm^2 square, fig 3.8(a). The uncertainty of the initial positioning makes the scanning speed of the STM/AFM the second factor which makes the localization of a specific NW nontrivial.

The maximum scanning speed is 200 nm/s, any faster and the tip will be damaged as it will "crash" into the leads, guiding pattern, or the actual NW itself. Tuning the feedback loop to be fast enough to handle larger scanning speeds (i.e. not "crashing") will result in an unstable feedback loop which in turn makes the tip move uncontrollably up and down. This makes imaging (of these samples) at speeds larger than 200 nm/s impossible. At 200 nm/s, a 4x4 μm^2 image with 50 nm resolution (low resolution) will take roughly half an hour to record. To cover an area of 100x100 μm^2, it would take almost two weeks of constant scanning night and day, which is not a feasible timescale for these experiments. The guiding pattern, seen in fig 3.8(a) and more clearly in fig 3.8(b), as vertical lines, were made to tremendously decrease the time needed to find a specific NW. With the guiding pattern in place, the tip can, with high probability, be placed on top of the guiding pattern area that is corresponding to the externally connected NW of

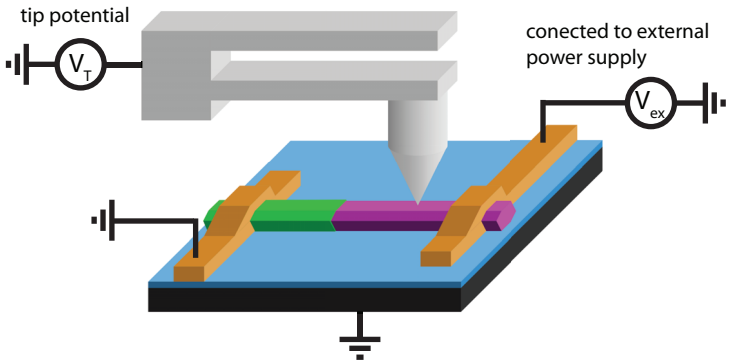

Figure 3.9: Schematic presentation of the set–up used for our SPM measurements. The NW is contacted with the golden leads which, in turn, are connected to the external power supply. The power supply is used to apply a potential to one end of the NW during the STM measurements, but it is also used to measure the conductance when performing SGM. The tip mounted on the tuning fork (to enable AFM mode) is also shown.

interest. The lines in the guiding pattern have different width depending on which side of the NW they are situated. From a single line scan, with the length of 10 μm, on top of the guiding pattern, it is then possible to determine which side of the NW the tip is. From there one carefully moves the position of the tip to where the lines change their width and then proceed up until the marker area ends. It is not necessary to record full images until the next step in locating the NW which saves much time. From here typically one or two 4x4 μm^2 images are enough to locate the NW, fig 3.8(b). With this procedure the time it takes to localize a specific NW is reduced to one to three hours.

Once the NW is located, and the tip is placed on top of the NW surface the actual STM investigations of the NW device can commence, fig 3.9. Here it is critical to stay on the NW because any scanning in STM mode on the SiO_2 will result in severe deterioration of the tip. When the NW surface is clean, and no oxides are present, the structure of the NW surface can be studied at the atomic scale. Especially interesting would be to study the migration of vacancies and adatoms when the NW is biased. Unfortunately, in Paper **I** this was not achieved due to a very persistent oxide layer. The combination of the system materials and the overall device design put limitations on the cleaning procedure. The materials of the NWs require higher temperatures to become clean than the leads can handle. At higher temperatures the NWs break eliminating any possibilities for measurements. Ongoing work with different device designs will, however, solve both the issue of the surface oxide removal and also altogether remove the need to use the AFM to locate the NWs.

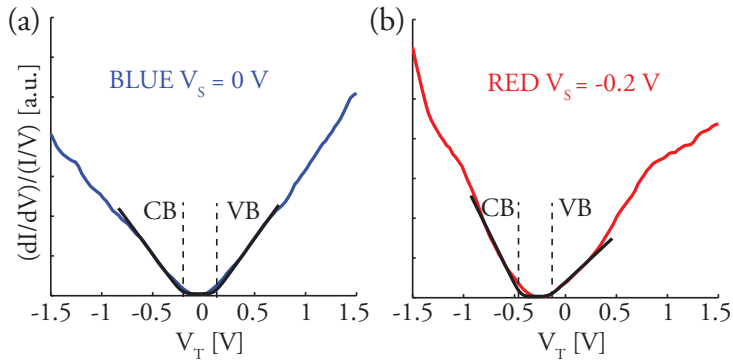

Figure 3.10: STS spectra recorded on a contacted NW for different applied potential to the NW (V_S). (a) STS spectrum recorded while the NW was grounded. The conduction band edge, CB, as well as the valence band edge, VB, are shown as black dashed lines. (b) Shows STS spectrum recorded at the same position on the NW but with an external potential of 0.2 V applied to one end of the NW. Here the change in the conduction- as well as the valence band edge is seen.

Even without atomic resolution, however, the surface density of states of the NW can be mapped with nm resolution and in Paper **I** it is also shown that the local potential on the surface of the biased NW corresponds to the potential inside the NW. The change in potential along the biased NW is determined by comparing STS spectra recorded along the NW when it is biased (with the external power supply) with spectra recorded when the NW is grounded. The onset of the conduction- and valence band edge will change between the compared spectra, and the change corresponds directly to the potential at the NW surface, fig 3.10. For clarity, picture the simpler case where one is performing STS on a metal sample. There will be a tunneling current between the tip and the sample for all tip-potentials, V_T, except for when the potential difference between the tip and the sample is zero. If the sample is grounded, a minimum in the STS spectrum will be seen at $V_T = 0$. For any sample potential, V_S, the minimum will be found at $V_T = V_S$.

The same experimental set-up used to perform STM on NW devices can also be utilized to perform scanning gate microscopy (SGM). In SGM the electrical conductance of (in this case) the NW is measured as a function of the tip position and potential. In Paper **II** this is shown where we, instead of performing STM on the NW, scan on top of the NW with a constant potential on the tip using the AFM feedback signal. By simultaneously measuring the conductance through the NW itself, using the external power supply (fig 3.9), and correlating this with the tip position we create a map of the NW showing how the conductance through the NW changes depending on where it is gated.

3.4 STM top contact mode

A large part of the work behind this thesis has been spent on development and, in turn, the use of the technique which I have chosen to call STM top contact mode. The development of new characterization methods for electronic properties of NWs is crucial for the continued development of NW devices. The existing methods include NW FET geometry [42, 80, 81] as well as using different types of nanoprobes. *I-V* characteristics for a variety of NWs with different material compositions could be revealed by using a metal nanoprobe inside a scanning electron microscope (SEM) [82-88]. This method requires a UHV compatible SEM to avoid carbon contamination of the samples investigated. In Paper **III** we presented our novel technique, STM top contact mode, where we instead utilize a standard STM both for imaging and contacting upstanding NWs for electrical characterization. In Papers **IV** and **V**, we then continue our research and utilize the technique for further investigations of NWs. With STM top contact mode there is no need for an SEM since the STM can be used both to locate the NWs and to position the probe (in this case the STM-tip). The tunnel current signal is used to carefully position the STM-tip (nanoprobe) at the NW, which is a more sensitive way than controlling the nanoprobe position according to the information from an SEM image. If the STM is used under UHV conditions, the contact between the STM nanoprobe and the top end of the NW can be ohmic.

STM top contact measurements are highly different from standard STM measurements. The goal is to create a point contact between the NW and the STM tip to enable measurement of the NW conductance. Thus, there is no tunneling current between tip and NW when the conductance measurements are conducted. A special approach has to be adopted when investigating up-standing NWs because of their extreme geometry which is not compatible with standard STM imaging. Without special considerations the NWs will simply break of the substrate and the tip will be irreversibly damaged. The procedure when performing STM top contact measurements is as follows:

The first step is to locate the upstanding NWs without damaging either NWs or tip. For this, the standard auto-approach of the STM can be used to bring the tip close to the surface of the sample. Either the tip will reach the substrate, or it might stop before that if it is close to a NW, fig 3.10(c), depending on the density of NWs on the sample, the height of the NWs, and the shape of the tip. A general rule of thumb is that the tip may reach the substrate if the average distance between NWs on the sample is larger than half the NW height. This has to be kept in mind during the next step which is the retraction of the tip. If there is any uncertainty whether the tip has reached the substrate during the auto-approach or not, the tip has to be retracted a distance larger than the height of the NWs. If one

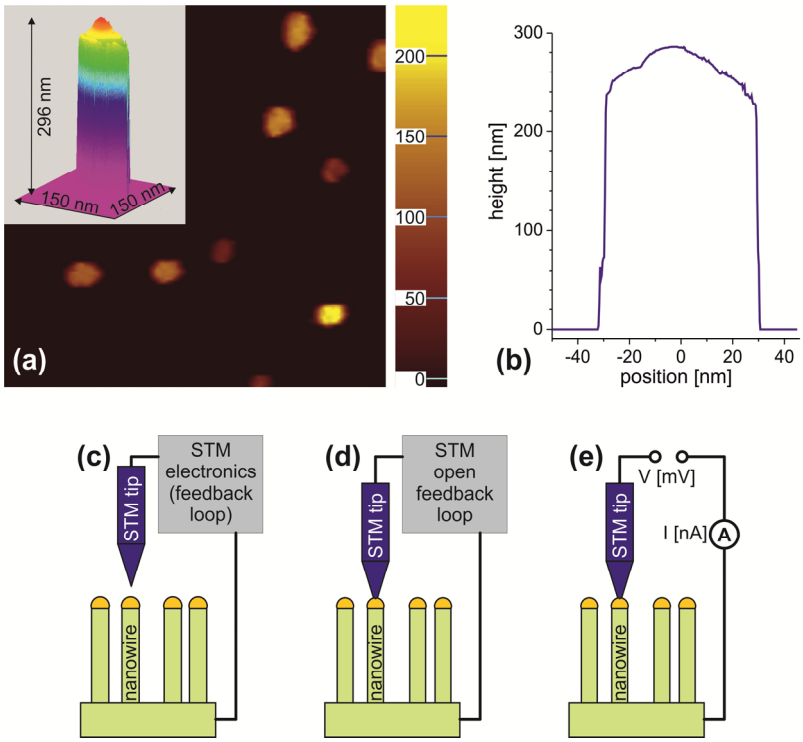

Figure 3.10: (a) A 1 μm^2 STM image showing the top of several InAs NWs (color scale in nm). The STM tip does not reach the substrate; it is limited by the piezo range, and the black areas between the NWs is the tip scanning in vacuum without any tunneling current. The inset is a 3D rendering of one NW as imaged by the STM. (b) Height profile of the inset in (a). (c-e) Schematic view of the STM point contact procedure. (c) Scanning to find a NW. (d) Immersing the tip in the top metal particle. (e) Measurning the *I-V* characteristics with an external current amplifier. Image adopted from Paper **III**.

is certain that the tip did not reach the substrate during the auto-approach, a considerable amount of time will be saved during the next step by adjusting the retraction distance. Now the search for NWs can commence. One starts of by defining a scan area large enough to, on average, find at least one NW and then proceeds to record an image. If the precursory steps have been performed correctly, nothing will be seen on this first image since the tip will be scanning in mid vacuum. After the initial image, the tip can be moved closer to the sample (100 nm is standard, but differences in NWs and tips can increase or decrease this distance) and another image is recorded. This procedure is repeated until the top ends of the first NWs are seen in an image, fig 3.10(a). Each image recorded might take a considerable time to record (3x3 μm^2 with 20 nm resolution at 150 nm/s will take 50 min) so the fever the steps one has to take before the NWs are

reached the better. This approach method has been reported on earlier, and a more specific description can be found in ref. [89]. It should be noted that with this procedure also samples with insulating layers can be used. As long as the NWs are close enough together the STM will only see the top of the NWs which typically is comprised of a metal nanoparticle.

Once a NW has been localized the top can be imaged, and its height profile can be determined, fig 3.10(b). This ensures that the tip is centered above the middle of the NW top metal particle where the point contact is to be established. The tip is placed over the NW, and the STM feedback loop is disconnected to allow the tip to be pressed onto the top particle, fig 3.10(d), as the tip approaches the NW. The point contact formation is detected as a strong increase in current. The current is no longer a tunneling current, and the amount is too large for the STM electronics, exceeding its saturation limit, and an external current amplifier with larger range is connected, fig 3.10(e).

All NWs studied in Papers **I-V** are grown by Au-particle-assisted growth with Au particles with a diameter of 50 to 170 nm. STM tips etched in our lab typically have a radius of curvature which is less than 30 nm. The contacting between the W tip and the NW is thus a metal to metal contact. At first contact, the cross section of the tip touching the Au particle is small enough to limit the current density through the formed circuit. However pressing the tip further towards the Au particle will form an ohmic contact with orders of magnitudes lower resistance than the NWs studied. For the *I-V* characteristic measured to be dominated by the NW and top Au particle characteristics and not the rest of the circuit, it is of utmost importance that the contacts are ohmic. This is ensured in STM top contact mode since the NW is only contacted via the crystalline NW–growth substrate (which is highly doped) interface and the ohmic contact between the STM tip and the top Au particle.

STM top contact mode is performed in UHV conditions giving control over the sample surface conditions. It also enables the possibility to remove the surface oxides of the NW side facets as described in chapter 2.6 which is shown in Paper **IV**. The UHV conditions also enable sputtering of the tip assuring an oxide free probe and enabling the ohmic contact between the tip and the Au top particle of the NW. The STM set-up allows for subnanometer resolution and positioning and the exclusion of additional sample processing making the technique very versatile.

Further development of this technique is undergoing, and in the spring of 2017, a combination with the STM top contact mode and a nano-diffraction beamline will enable further investigation possibilities. By establishing a point contact to an individual NW placed perpendicular to the beam correlations between single NW

crystal structure and *I–V* characteristics can be measured. It will also be possible to follow current-induces structural defects live.

3.5 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a technique pioneered by K. Siegbahn (for which his was awarded the noble prize in 1981) and co-workers [90] and it is a powerful tool for characterization of both the chemical and the electronic structure of surfaces. In Papers **VI** and **VII**, we utilize this tool to investigate the structure of HfO_2 and how it is formed. XPS uses monochromatic light to excite electrons (photoelectrons) from a sample. The kinetic energy of the emitted electrons is detected which in turn can give the original binding energy of the electrons in the sample. The binding energy is correlated to various characteristics of the sample. The development of the technique and the introduction of synchrotron radiation, especially the third generation synchrotrons with insertion devices, has allowed for higher resolution and faster experiments over the years. Regular XPS is a surface sensitive technique with a probing depth of a few nm. The emitted electrons will not escape from deeper in the sample, without losing kinetic energy, due to the photon energies used in XPS. However, in 2003, Kobayashi et al. [91] showed that XPS could also be used for probing deeper into materials using higher photon energies, which give higher electron kinetic energies. Electrons with higher kinetic energy will be able to travel further in the sample without losing kinetic energy enabling deeper probing depths. The technique has many abbreviations; in this thesis we call it hard X-ray photoelectron spectroscopy (HAXPES). The use of new high brilliance undulators (10^{11} photon/s) and also analyzers that can handle electrons with kinetic energies up to 15 keV has been vital for the development of HAXPES. Depth profiling of samples has been shown by measuring the intensity of core level photoelectrons, either at different excitation energies [92] or at different take–off angles [93]. In Paper **VI** we utilize the technique with different excitation energies to probe the HfO_2 layer and determine its homogeneity, and we can also analyze the underlying InAs (through a layer of metal and a layer of HfO_2) and see a strong reduction in the native As oxide. The working principles for HAXPES are still the same as for XPS, with the exception that HAXPES allows for investigations deeper into your sample.

All XPS and HAXPES work conducted during the time span of this thesis has been done using synchrotron light sources. A synchrotron light source consists of a particle accelerator for electrons and a so–called storage ring. In the storage ring, the electrons travel at near the speed of light and as they are accelerated normal to their trajectory they emit photons. This is done both by the bending magnets that

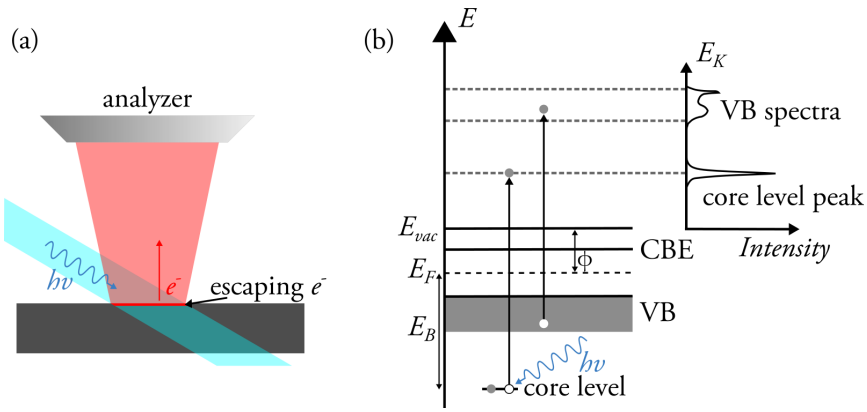

Figure 3.11: (a) Simplified image of the XPS set-up showing the photons penetrating the sample but only electrons escaping from the top most layer reaching the analyzer without losing energy. (b) Schematic description of the processes involved in the recording of an XPS spectrum. The electrons will be excited from core levels and the valence band (VB) giving rise to various features in the recorded spectrum. The kinetic energy of the detected photoelectrons will depend on the energy of the photons ($h\nu$), the electron binding energy (E_B) and the sample work function ϕ. E_B is given with respect to the Fermi level which for semiconductors typically is in the band gap between VB and the conduction band edge (CBE).

keep the electrons on their circular path, but more importantly by insertion devices (undulators and wigglers) which can produce photon beams with very high intensities and well-defined energies, which are highly collimated and polarized. The photons produced by the synchrotron light source are then used to excite electrons in a sample according to the photoelectric effect explained by Einstein in 1905 [94]. The electrons will leave their bound state, travel through the sample, into the vacuum in the analysis chamber, and reach the electron kinetic energy analyzer. The intensity of the electrons is then typically displayed as a function of their binding energy which is related to their kinetic energy as described in chapter 3.5.2. Due to interactions between the electrons and the sample, only electrons excited in the uppermost layer of the sample will reach the detector unaffected, fig 3.11(a). This is the reason why XPS is a surface sensitive technique, but as discussed above this can be circumvented by using photons with higher energies (HAXPES) because the amount of interaction between the electrons and the sample is dependent on the kinetic energy of the electron.

3.5.1 Theory

A sample analyzed with XPS can be seen as a system containing N electrons, fig 3.11(b). When the sample absorbs a photon with energy $h\nu$ and emits an

electron with kinetic energy E_K, the energy of the system changes and can be described as

$$E_i(N) + h\nu = E_f(N-1) + E_K, \quad (3.10)$$

where $E_i(N)$ is the initial energy state and E_f is the final. The energy it takes to remove an electron from an atom in the sample (ionization potential) can then be derived as $E_f(N - 1) - E_i(N)$ or as the energy difference between the incoming photon and kinetic energy of the emitted electron.

The electron analyzer typically detects the kinetic energy of the photoelectrons by measuring their deflection in an electric field. To get information on the studied sample, the binding energies E_B of the electrons are needed. The binding energy is the ionization potential minus the work function ϕ of the sample,

$$E_B = h\nu - E_K - \phi. \quad (3.11)$$

The work function is the minimal energy needed to excite an electron of a solid into vacuum and it is not a bulk specific property, but it is also dependent on the sample surface. Herein lies a problem since the photoelectron has to be detected as well. In fact, E_K will be measured with respect to the vacuum level of the analyzer and not the sample. The Fermi levels of the sample and the analyzer are connected via ground and are thereby at the same level, but the vacuum levels are not. Provided we know the energy of the photons, we can calculate E_B of the photoelectrons only with the systematic error of the difference in ϕ of the sample and the detector. This uncertainty, however, is in the order of a few eV and relevant core level peaks in XPS spectra are typically rather straight forward to identify (of course depending on the complexity of your sample). When comparing spectra recorded at different times, a point of reference is needed to ensure that one compares the absolute energy values. This reference can be the valence band edge when studying metals (i.e. the Fermi level). For semiconductors, on the other hand, a well-defined core level peak is often used because the electron distribution at the valence band edge is harder to evaluate.

In a solid, the valence electrons are the electrons forming the chemical bonds between the atoms. They also make up the partially filled outer shell of an atom and are relatively close to the vacuum level. There are many (a band of) energy states which these electrons can occupy. The valence electrons in solids are shared between the atoms and in metals they are completely delocalized. For semiconductors, they are shared between neighboring atoms. The core electrons, on the other hand, are localized to a specific atom and have confined energy levels which are element specific. The binding energy of the core electrons are however not completely unaffected by the

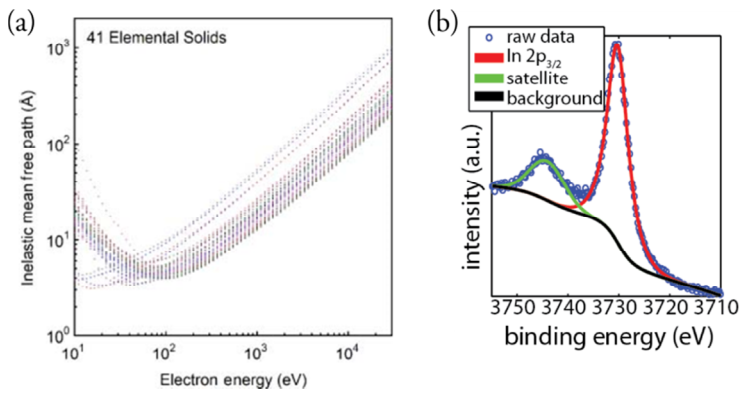

Figure 3.12: (a) The calculated IMFP for 41 different solids as a function of electron kinetic energy. Image adopted from ref. [95]. (b) Typical HAXPES spectrum showing one of the spin–orbit splitted In *2p* core level peak (the In $2p_{3/2}$) and satellite peak. Blue circles are the raw data, red line the fitted main peak (In $2p_{3/2}$), green line the fitted satellite, and the black line is the fitted background.

surroundings and can vary due to different valence state conditions, more in chapter 3.5.3.

Upon interaction between the photon and electron, the chance for an excitation to take place is described by the photoionization cross section of the atomic subshells, and it typically declines with increasing excitation energy. This decrease in cross section at the high photon energies used for HAXPES introduces a drawback which can partially be circumvented by investigating deeper lying core levels. These levels have higher photoionization cross sections at high excitation energies compared to more shallow levels [96]. Fortunately, these deeper lying core levels are also possible to ionize due to the high photon energies used.

3.5.2 Inelastic mean free path

The ability of an electron to travel through its surroundings unaffected can be described with the inelastic mean free path (IMFP). It is simply a measurement of how far an electron can travel in a certain material without losing kinetic energy. The IMFP is defined as the distance a beam of electrons, with a certain energy, will travel before its intensity is down to 1/e (37%) of the original intensity. At kinetic energies larger than 100 eV (which is the case for all electrons studied in this thesis) the IMFP increases with energy, fig 3.12(a). The intensity I of the electrons that has maintained its energy E after traveling a distance d in a solid can be described as

$$I(d) = I_0 e^{\frac{-d}{\lambda(E)}}, \quad (3.12)$$

where I_0 is the original intensity, and λ is the IMFP. There are many processes contributing to the energy loss of the electron. The main three (detectable in XPS measurements) are, plasmon scattering, single-particle electron excitations involving valence electrons, and ionization of core levels of the atom which compose the solid [97]. At energies below the plasmon energy, scattering is dictated by single particle excitations. Although the IMFP is different for different materials, a good rule of thumb is that an electron with kinetic energy measured in keV has the same IMFP in nm, fig 3.12(a).

Although the surface sensitivity of XPS can be derived from the IMFP of electrons (1 nm at 1 keV), that is not the whole truth. Here it is prudent to point out that there are also elastic scattering events affecting the electrons on their way to the surface. The elastic scattering processes in themselves do not influence the electron energy, but they have the effect that they increase the average path the electrons travel. This will make the electrons lose more energy on their way to the surface, due to inelastic scattering, than it would do were there no elastic scattering. The accordingly corrected distance is called the electron attenuation length, and it can be as much as 30% shorter than the IMFP [97].

The IMFP also plays a role after the electron has exited the solid. As mentioned above it is crucial to maintain UHV conditions during XPS studies allowing for the electron to reach the electron kinetic energy analyzer. Because even though the IMFP for an electron in a gas is many orders of magnitude longer than in a solid, it is still proportional to the gas pressure and at 1 mbar it is in the order of 10 mm [98], depending on the kinetic energy of course. At UHV conditions ($< 10^{-9}$ mbar) the IMFP can be longer than 10^4 km.

3.5.3 Analyzing HAXPES spectra

The XPS spectrum displays the collected electrons as a function of their binding energy. Although core levels are localized, and core electrons do not contribute to the chemical bonds in the sample, changes in the initial or final state (see below) of the valence levels will affect the core electron binding energy. With proper analysis of the obtained spectrum, chemical information can be gained from these changes of the binding energies. The analysis of HAXPES spectra is very similar to the analysis of XPS spectra. The main difference is the background which is even more pronounced at the higher photon energies used during HAXPES.

The photoemission process in XPS can be seen as a three-step process:

1) Absorption of a photon by an atom in the sample and ionization (initial state effects).

2) The response of the atom and the emission of an electron (final state effects).

3) Electron traveling to the surface and escaping into vacuum (extrinsic losses)

All of these effects contribute to the appearance of the XPS/HAXPES spectrum. The two most important initial state effects for the work in this thesis are spin-orbit splitting and chemical shifts, but also charging of the sample and Auger electrons influence the XPS spectrum.

Spin-orbit splitting occurs for all core levels with electrons that have an orbital angular momentum and is seen as two peaks rather than one for those core levels. The coupling between the magnetic fields from the electron's spin (s) and its angular momentum (l) can be either favorable or unfavorable, and the total angular momentum (j) is expressed as $j = |l \pm s|$. Electrons in s orbitals have no angular momentum and hence corresponding core levels have no spin-orbit splitting. The p, d, f… orbitals, on the other hand, have, and hence those core levels are split into two. The spin-orbit coupling increases for atomic orbitals closer to the nucleus resulting in larger spin-orbit splitting for corresponding core levels. Typically for HAXPES only one of the spin-orbit split core level peaks is recorded, fig 3.12(b), due to the large spin-orbit splitting of the lower core levels investigated, see chapter 3.5.2.

The positions of orbitals in an atom are sensitive to their chemical environment. The core level peak will be changed in binding energy if the overall charge of the atom is changed. This chemical shift is typically seen as a change in binding energy, for example between a core level for an element in its elemental form and its oxidized form. The oxygen atoms attract electrons making the overall charge of the oxidized, e.g. Hf, atom greater and in effect binding the core electrons stronger, shifting the Hf core level peaks towards higher binding energies.

The final state effects are caused by various atom relaxations associated with the photoelectron emission. The electron-hole creation may excite another electron to a bound state with higher energy; the photoelectron will then lose kinetic energy with the same amount causing a peak shift to higher binding energies, *shake-up satellite*. These peaks are normally shifted by 1-10 eV higher with respect to the main peak [99]. The core-hole creation can also excite an electron into vacuum, *shake-off satellite*. This will produce a peak at higher binding energies than the shake-up and with wider energy spread as well [100].

On its way through the sample, the photoelectron may also lose kinetic energy referred to as extrinsic losses. All XPS spectra show a stepped background, fig 3.12(b), where the intensity of the background increases on the higher binding energy side of a core level peak due to the inelastic scattering of the electrons

emitted from within the sample. Only electrons generated up to one IMFP into the sample, on average, can escape the sample without any loss of kinetic energy. The background can be fitted with a Shirley function to remove the asymmetry the stepped background introduces to the core level peaks [101]. Plasmon excitations are also seen when the photoelectrons introduce a collective quantized excitation of the free electron gas at the Fermi level, creating peaks at 10-30 eV higher binding energy [97] than the main peak.

All these physical phenomena described above will give rise to different peaks and features in the XPS spectrum. But the situation described above is the ideal case. In reality, all peaks will also be broadened because of instrumental limitations and the short lifetime of the core hole. Instrumental broadening is due to the energy width of the excitation photons, which in turn is limited by the monochromator used and its resolution, and the analyzer resolution. The monochromator resolution will go down with increased excitation energy while the analyzer resolution is independent of excitation energy. The instrumental broadening can be described with a Gaussian distribution. The life time of the core holes will also influence the width of the peaks due to the relation derived from Heisenberg's uncertainty principle, namely that the lower the lifetime is, the broader the energy spread is. The lifetime is inversely proportional to the binding energy so that core levels at higher binding energies will have a broader peak width. The lifetime broadening can be described with a Lorentzian distribution. Together the instrumental (Gaussian) and lifetime (Lorentzian) broadening will give a symmetrical broadening of the peaks in the XPS spectrum which can be modeled with a Voigt distribution function.

The excitation energy dependence of the monochromator and the lifetime dependence on binding energy both degrade the optimal resolution that can be achieved with HAXPES compared to XPS. For the HAXPES measurements performed at ESRF, presented in Paper **VI,** a resolution of 2 eV at 11 keV excitation energy was achieved.

3.5.4 Ambient–pressure XPS

Ambient–pressure XPS (APXPS) is a development of the standard XPS where the sample can be kept at relatively high pressure (in the mbar range) [102]. This enables measurements of chemical reactions at surfaces when they are exposed to gasses. This is not possible with standard XPS due to the UHV conditions required for standard XPS. There are different experimental set-ups that enable APXPS but they all have a common denominator, the differential pumping system before the electron analyzer, fig 3.13. Separate turbopumps enable the electrons

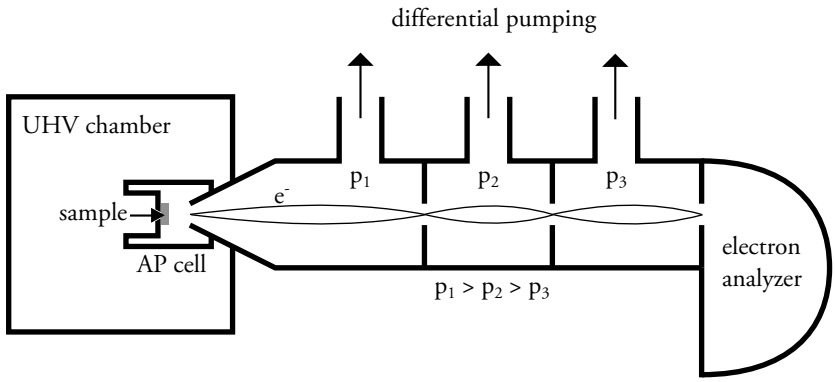

Figure 3.13: Schematic drawing of the APXPS Lund approach. Here the ambient pressure (AP) cell is shown where the sample is placed to enable the much higher pressures compared to standard XPS. The differential pumping system is also shown which is needed for the electron to reach the electron analyzer. It is also essential to keep the low pressure needed inside the analyzer.

emitted from the sample to reach the electron analyzer without losing kinetic energy.

In Paper **VII** we utilize APXPS to reveal the growth process of HfO_2 on InAs substrates. The set-up used by us to perform APXPS experiments is called the Lund approach [103]. Here, a small ambient pressure cell (where the sample is kept) is inserted into the UHV chamber, fig 3.13. The ambient pressure cell acts as a flow reactor with connections to external gas lines. This enables chemical reactions to take place under constant conditions as well as easy purging of the gasses due to the relatively small volume of the cell. These features combined make it possible to implement the ALD process within the cell which in turn enabled us to study the process in detail.

4 Concluding remarks and outlook

The focus of the work presented in this thesis is on the development and utilization of non-destructive, surface sensitive, and in some cases, novel characterization techniques. The goal is to increase the understanding of current NW devices and help in the development of new and better devices.

Most of my research, in the beginning, was focused on the development of the top contact method. Our group had already started developing this technique before I started. The standard pre-amplifier in an STM typically can not handle the currents produced with this technique once the STM-tip is in contact with the NWs. This limits the STMs available, to use for this technique, to STMs where the pre-amplifier is easily replaceable, i.e. STMs with external pre-amplifiers. After years of developing the technique, we now have a new system which can routinely make these measurements. In Paper **III-V** the results of our investigations are presented. Paper **III** and **V** are based on data recorded mostly with our old set-up and Paper **IV** is based on data from the new set-up. This novel method has the advantage of being extremely clean which allows the formation of good ohmic contacts between tip and NW. It also enables surface treatment of the NW surfaces, such as cleaning and re-oxidation. In the future, I can see this method utilized as a common tool for NW characterization. Further development is undergoing, and in the spring of 2017, a combination with the STM top contact mode and a nano-diffraction beamline will enable further investigation possibilities. This will make it possible to correlate single NW crystal structure with the *I–V* characteristics, as well as following current-induced structural defects live.

A lot of my time has also been spent on "beam times" on different synchrotron radiation facilities around the world. Some of the results from these are presented in Paper **VI** and **VII** where the high-k dielectric oxide HfO_2 is studied in scrutinizing detail. Here we can show that the quality of the critical interface between HfO_2 and InAs is dependent on the first half-cycle of the ALD process where the TDMA-Hf precursor is responsible for the removal of the native InAs-oxide. By revealing the nature of the ALD process of HfO_2 on InAs, better transistors will hopefully be realized.

Developing the technique to study contacted NWs in FET configuration with STM was also a big part of my research. Although atomic resolution was not achieved with our first experiments, detailed information on the electronic behavior of the NWs where revealed and presented in Paper **I** and **II**. Ongoing development of drastically different sample designs has moved our focus slightly away from the AFM/STM approach. Now atomic resolution can be achieved on contacted NWs with a standard STM. Further research in this area is ongoing and new results will be published in the near future. However, the AFM/STM approach is still relevant because it allows for studies of standard NW devices.

Fourth generation synchrotron radiation light sources are built around the world and with their help researchers will continue to push the boundaries of what is possible to resolve with various X-ray techniques, both in time and space. AFM, STM, and STS are very good complementary techniques to the techniques implemented at these new synchrotron radiation light sources.

I see a bright future for the continued research with our explored methods. There is still much to discover with regards to the electric characteristics of NWs and how these are affected by different crystal structures as well as surface properties. We have shown how oxidation of NW surfaces can both increase and decrease the conductance of NWs, but many other relevant experiments are left to be explored. The study of adsorption of molecules on NW surfaces could pave the way for many new applications. The increasing understanding of the mechanisms behind NW growth could also enable completely new material combinations as well as structures. For example, NWs as topological insulators have already been shown and the research about Majorana fermions is ongoing.

Science moves forward and the knowledge about NWs, NW devices, and their surfaces are only increasing with time. The properties of NW devices are, in large part, dictated by the atomic structure of their surfaces and interfaces. Faster and more power saving transistors, as well as superior solar cells, are just a few examples of the improvements our research will hopefully lead to. My hope and feeling are that we have, with our unrelenting research presented in this thesis, helped science a bit on its way (hopefully more than a couple of nm!).

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6 Summary of papers

I. Scanning Tunneling Spectroscopy on InAs–GaSb Esaki Diode Nanowire Devices during Operation

We demonstrate stable scanning tunneling spectroscopy (STS) with nanoscale resolution on electrically active nanowire devices in the common lateral configuration using a combined scanning tunneling and atomic force microscope in conjunction with in-vacuum atomic hydrogen cleaning. We use this method to map out the surface density of states on both the GaSb and InAs segments of GaSb–InAs Esaki diodes as well as the transition region between the two segments. Generally, the surface shows small band gaps centered round the Fermi level, which is attributed to a thin multi-element surface layer, except in the diode transition region where we observe a sudden broadening of the band gap. By applying a bias to the NW, we find that the STS spectra shift according to the local nanoscale potential drop inside the wire. Importantly, this shows that we have a nanoscale probe with which we can infer both surface electronic structure and the local potential inside the NW, and we can connect this information directly to the performance of the imaged device.

II. High Resolution Scanning Gate Microscopy Measurements on InAs/GaSb Nanowire Esaki Diode Devices

Here, we present a study by SGM of newly developed III–V semiconductor NW InAs/GaSb heterojunction Esaki tunnel diode devices under ultra-high vacuum. Sub-5 nm resolution is demonstrated at room temperature via the use of quartz resonator atomic force microscopy sensors, with the capability to resolve InAs nanowire facets, the InAs/GaSb tunnel diode transition, and nanoscale defects on the device. We demonstrate that such measurements can rapidly give important insight into the device properties via the use of a simplified physical model, without the requirement for extensive calculation of the electrostatics of the system. Interestingly, by precise spatial correlation of the device electrical transport properties and surface structure we show the position and existence of a very abrupt (<10 nm) electrical transition across the InAs/GaSb junction despite the change in material composition occurring only over 30–50 nm. The direct and simultaneous link between nanostructure composition and electrical properties

helps set important limits for the precision in structural control needed to achieve desired device performance.

III. Current-Voltage Characterization of Individual As-Grown Nanowires using a Scanning Tunneling Microscope

We report accurate on-top imaging and *I-V* characterization of individual as-grown nanowires, using a subnanometer resolution scanning tunneling microscope with no need for additional microscopy tools, thus allowing versatile application. We form ohmic contacts to InP and InAs nanowires without any sample processing, followed by quantitative measurements of diameter dependent *I-V* properties with a very small spread in measured values compared to standard techniques. Supporting information on initial results for NW *I-V* changes as response to surface cleaning is also reported.

IV. The Effect of Surface Oxide and Wurtzite/Zinc blende Interfaces on the Conductivity of InAs Nanowires

Here we show how the conductivity of InAs NWs is affected by the surface states of the NW side facets. Our developed top contact method is used to investigate the conductivity of InAs NWs with different crystal structures. A decrease in conductivity and an increased rectifying behavior is seen for InAs NWs with pure wurtzite crystal structure when the surface oxides of the NWs are removed. InAs NWs comprised of one segment with wurtzite crystal structure and one with zinc blende, on the other hand, show the opposite effect; the conductivity goes down, and the behavior becomes ohmic with oxide removal. With our set-up, re-oxidation and subsequent re-cleaning is possible, and it shows that the effects are also reversible proving that it is indeed the surface oxide removal that is responsible for the changes seen.

V. Strong Schottky Barrier Reduction at Au-Catalyst/GaAs-Nanowire Interfaces by Electric Dipole Formation and Fermi-level Unpinning

We report the realization and characterization of low n-type Schottky barriers (~0.35 eV) formed at epitaxial contacts between Au-In alloy catalytic particles and GaAs-nanowires. In comparison to previous studies, our detailed characterization, employing selective electrical contacts defined by high-precision electron beam lithography, reveals the barrier to occur directly and solely at the abrupt interface between the catalyst and nanowire. We attribute this lowest-to-date-reported Schottky barrier to a reduced density of pinning states and the formation of an electric dipole layer at the epitaxial contacts. The insight into the physical

mechanisms behind the observed low energy Schottky barrier may guide future efforts to engineer abrupt nanoscale electrical contacts with tailored electrical properties.

VI. Interface Characterization of metal-HfO2-InAs Gate Stacks using Hard X-ray Photoemission Spectroscopy

We studied the interface structure and chemical composition of realistic MOS gate stacks, consisting of a W or Pd metal film and a 6- or 12-nm-thick HfO_2 layer deposited on InAs, with Hard X-ray Photoemission Spectroscopy. In and As signals from InAs buried more than 18 nm below the surface were clearly detected. The HfO_2 layers were found to be homogeneous, and no influence of the top metal on the sharp InAs-HfO2 interface was observed. The results bridge the gap between conventional photoemission spectroscopy studies on various metal-free model samples with very thin dielectric layers and realistic MOS gate stacks.

VII. Self-cleaning and Surface Chemical Reactions during HfO_2 Atomic Layer Deposition on InAs

For the first time we directly experimentally verify the chemical reactions at the surface during the first ALD cycle of HfO2 on InAs under realistic synthesis conditions using XPS. We find that the widely used ligand exchange model of the ALD process for the removal of native oxide on the semiconductor and the simultaneous formation of the first HfO2 layer must be revised. Our study provides substantial evidence that the efficiency of the ALD self-cleaning process and the quality of the resulting III-V semiconductor-oxide interface, can be controlled by the molecular adsorption of suitable ALD precursors, rather than the following high-k oxide formation.