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Sub-100-nm Gate-Length Scaling of Vertical InAs/InGaAs Nanowire MOSFETs on Si

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Abstract—We demonstrate a process to vary the gate-length of vertical MOSFETs on the same sample with high accuracy and high performance. Fabricated vertical InAs/InGaAs MOSFETs on Si have gate length ranging from 25 nm to 140 nm. The results shown are from single nanowire transistors as well as arrays with nanowires ranging from 80 to 500 nanowires. The devices show good yield and clear scaling trends. We demonstrate a device with gate-lengths comparable to the state-of-the-art lateral III-V MOSFETs.

I. INTRODUCTION

Vertical MOSFETs are considered to extend the transistor scaling at the extremely scaled nodes. Technology comparison has shown, that the vertical structure offers improved performance at the extremely scaled nodes as more space is available for contacts and spacers, when compared to FinFETs and laterally stacked gate-all-around (GAA) MOSFETs [1]. Vertical nanowire structure further allows integration of high-mobility materials on Si due to the possibility to relax stress originating from the lattice mismatch. Several demonstration of vertical MOSFETs have been published [2-7], however so far vertical MOSFETs with scaled gate-lengths have not been demonstrated. It is necessary to scale the gate-length, even though the gate-length in vertical MOSFETs is decoupled from the footprint, in order to improve the performance.

In this work, we demonstrate vertical InAs/InGaAs heterostructure MOSFETs on Si with the gate length ($L_G$) down to 25 nm. The gate length is scaled from 25 nm to 140 nm showing clear scaling trends in all transistor metrics. By $L_G$ scaling and introducing a different drain contact metal, we manage to achieve $g_m = 2.4$ mS/µm and $I_{on} = 207$ µA/µm at $V_{DD} = 0.5$ V, which both are the highest values reported on vertical MOSFETs.

II. DEVICE FABRICATION

Illustration of the device fabrication and scanning electron micrographs (SEM) of the devices are shown in figures 1 and 2, respectively. The device fabrication is started by fabricating 300-nm-thick InAs source contact. The location of the drain contact can be controlled by the thickness of the sacrificial hydrogen silsesquioxane (HSQ) layer, which thickness can be altered within the same sample by changing the EBL dose [7]. The drain fabrication is started by spin-coating, EBL defining, and developing sacrificial HSQ layer in TMAH (25%). The process is followed by sputtering 20-nm-thick Mo layer and ALD depositing 3-nm-thick TiN. The metals are anisotropically etched and the HSQ removed, therefore leaving metal only on the sidewalls of the nanowires. The processing is followed by fabricating the HSQ bottom spacer. The thickness of the HSQ spacer can be, as well, controlled by the EBL dose, therefore allowing good spacer control, which makes possible the fabrication of gate-lengths as small as 25 nm. In this work, the bottom HSQ was 140-nm-thick and the position of the drain contact was increased, so that the gate-length was varied from 25 to 140 nm.

After the top part of the nanowire is covered by the drain metal and the bottom part by the HSQ spacer, the gate region is locally etched using digital etching. In other words, the gate region is oxidized in ozone and the formed native oxide removed by HCl. This etching is repeated until the highly doped shell is removed. A bilayer Al2O3/HO2 (ALD cycles 10/37) was deposited and followed by deposition of 50-nm-thick W gate metal. The device is completed by etching the excess gate metal, depositing organic (S1813) second spacer, and fabricating contacts.

III. RESULTS

Transfer and output characteristics of the device with 120 nanowires, diameter of 27 nm and $L_G = 75$ nm are shown in figures 3 and 4, respectively. The device has $g_m = 1.90$ mS/µm (normalized to the circumference) and $SS = 86$ mV/dec. Q-value ($g_m/SS) = 22 and $I_{on} = 407$ µA/µm at $V_{DD} = 0.5$ V, which are the highest reported on vertical....
MOSFETs. The device has the SS of $81 \text{ mV/dec}$ and $86 \text{ mV/dec}$ at $50 \text{ mV}$ and $500 \text{ mV}$, respectively, as shown in figure 5. The device shows good electrostatics by having $\text{DIBL} = 80 \text{ mV/V}$ at $1 \mu\text{A/µm}$ and reasonably low access resistance by having $R_{on} = 450 \text{ Ωµm}$.

Transfer and output characteristics of the single nanowire transistor with diameter of $37 \text{ nm}$ and $L_G = 45 \text{ nm}$ are shown in figures 6 and 7. The device shows record high $g_m = 2.4 \text{ mS/µm}$ in vertical MOSFETs and low $R_{on} = 340 \text{ Ωµm}$. However, due to the relatively large diameter and shorter gate-length, the device cannot be fully turned off, which cause $\text{DIBL} = 290 \text{ mV/V}$ at $50 \text{ mV}$ and $500 \text{ mV}$, respectively, as shown in figure 5. The device shows good electrostatics by having $\text{DIBL} = 80 \text{ mV/V}$ at $1 \mu\text{A/µm}$ and reasonably low access resistance by having $R_{on} = 450 \text{ Ωµm}$.

In figure 8, the transfer characteristics of the device with $80$ nanowires, diameter $28 \text{ nm}$ and $L_G = 75 \text{ nm}$ is shown. The device is biased in two different configurations, by having the drain at the top (bottom grounded) and by having the drain at bottom (top grounded). The device shows clear asymmetry by having one order of magnitude lower off-current and higher $g_m$ in the bottom ground configuration. The device also shows asymmetry in subthreshold behavior by having $SS = 91 \text{ mV/dec}$ in bottom ground configuration and $SS = 116 \text{ mV/dec}$ in top ground configuration. These differences are attributed to the location of the InGaAs, which is on the drain side on the bottom ground configuration and at the source side on the top ground configuration. The introduction of Ga reduces the probability for gate-to-drain tunneling. In addition, the contacts have asymmetry, which most likely slightly decreases performance in top ground configuration by having larger contact resistance on the source side.

Figure 9-14 show different transistor metrics versus the gate length. In figure 9, $g_m$ versus $L_G$ is shown. $g_m$ clearly increases, when the gate length is scaled, as expected. However, below $L_G = 45 \text{ nm}$, $g_m$ starts decreasing. This decrease is attribute to short channel effects, as well as a possible problem to fully gate the unintentionally doped channel. Figure 10 shows similar scaling of $I_{off}$, which behaves as expected. $I_{off}$ seems to stabilize below $100 \text{ nA/µm}$ at gate-lengths $75 \text{ nm}$ and larger. At smaller gate-lengths devices of this diameter cannot be fully turned off having $I_{off}$ well above $100 \text{ nA/µm}$. The heterojunction is expected to be at approximately $L_G = 50 \text{ nm}$, which together with longer gate-length explains the steep drop of the $I_{off}$ at $L_G > 50 \text{ nm}$.

In figure 11 $R_{on}$ versus $L_G$ is shown. In the figure, only devices with the seed particle of $28 \text{ nm}$ are shown, although devices with larger seed particle have slightly lower $R_{on}$. Dashed line shows a linear fit, where devices with $L_G = 25 \text{ nm}$ are excluded, as the $R_{on}$ seems to flatten at lower gate lengths. The increased resistance at shorter gate lengths could be attributed to un gated regions without channel doping. Extrapolating the linear fit, an access resistance of $212 \text{ Ωµm}$ can be determined. The access resistance is largely reduced from previously reported values, which could be attributed to the use of Mo top metal.

Figure 12 and 13 show $SS$ and $V_T$ versus gate-length. Both metrics show the expected scaling trend. $SS$ increases at the shortest gate lengths and $V_T$ decreases due to short channel effects. In figure 14, maximum intrinsic gain $(g_m/g_d)$ versus $L_G$ is shown. $g_m/g_d$ peaks at $L_G = 75 \text{ nm}$, as we are able to maintain good $g_d$ at low gate-lengths due to gate-all-around structure.

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IV. CONCLUSIONS

We have developed a process to vary the gate length of the vertical MOSFETs on the same sample and fabricate devices with gate-length as low as $25 \text{ nm}$. We demonstrate vertical InAs/InGaAs nanowire MOSFETs on Si with gate-length varying from $25 \text{ nm}$ to $140 \text{ nm}$. The devices show clear scaling trends. In addition, the devices have the highest $g_m = 2.4 \text{ mS/µm}$ and $I_{on} = 407 \mu\text{A/µm}$ at $V_{DD} = 100 \text{ nA/µm}$ and $V_{DD} = 0.5 \text{ V}$ than state-of-the-art vertical MOSFETs. However, state-of-the-art lateral InGaAs MOSFETs still show higher $I_{on}$ than the presently studied transistors.

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Fig. 1. Illustration of the process after top metal deposition (a), first spacer deposition (b) and final contacts (c). The gate-length can be controlled by controlling EBL dose in the top metal and bottom spacer fabrication.

Fig. 2. SEM of the device with $L_G = 25$ nm after high-$\kappa$ deposition (a). Completed device (b) has a large gate-drain overlap due to having different gate-lengths on the same sample.

Fig. 3. Transfer characteristics of the array with 120 nanowires, diameter 27 nm and $L_G = 75$ nm.

Fig. 4. Output characteristics of the array with 120 nanowires, diameter 27 nm and $L_G = 75$ nm.

Fig. 5. Subthreshold swing of the array with 120 nanowires, diameter 27 nm and $L_G = 75$ nm.

Fig. 6. Transfer characteristics of single nanowire transistor with diameter 37 nm and $L_G = 45$ nm.

Fig. 7. Output characteristics of single nanowire transistor with diameter 37 nm and $L_G = 45$ nm.

Fig. 8. Transfer characteristics of the array with 80 nanowires, diameter 27 nm and $L_G = 75$ nm. Measured in two different configurations (bottom and top ground).
Fig. 9. Mean and peak \(g_{m,\text{max}}\) of the devices with different \(L_G\).

Fig. 10. \(I_{\text{off}}\) of the devices with different \(L_G\).

Fig. 11. \(R_{\text{on}}\) of the devices with different \(L_G\). Extrapolation gives an access resistance of 212 \(\Omega\mu\text{m}\).

Fig. 12. Mean and peak \(SS_{\text{min}}\) of the devices with different \(L_G\).

Fig. 13. \(V_T\) of the devices with different \(L_G\).

Fig. 14. Maximum \(g_{m}/g_{d}\) with different \(L_G\).

Fig. 15. Unnormalized \(g_m\) versus number of nanowires in the transistor.

Fig. 16. The devices benchmarked versus the state-of-the-art vertical III-V MOSFETs.

Fig. 17. The devices benchmarked versus lateral and vertical III-V MOSFETs.