Efficient mm-Wave Transmitter Design in CMOS Technology

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2018

Document Version:
Publisher's PDF, also known as Version of record

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LUND INSTITUTE OF TECHNOLOGY
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Doctoral Dissertation
Lund, Sweden
2018

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ISSN 1654-790X, no.117
ISBN 978-91-7753-802-8 (print)
ISBN 978-91-7753-803-5 (pdf)
Series of licentiate and doctoral dissertations.

Produced using LaTeX Documentation System.
Printed in Sweden by *Tryckeriet i E-huset*, Lund.
November 2018.

Till min morfar
Arnold Meyer

Abstract

An increasing demand of higher data rates in wireless communication forces the industry to look to higher frequencies to find the required bandwidths. This thesis is about analog transmitters in CMOS for millimeter-wave communication, and it focuses on improving power amplifiers and frequency generation circuits, and increase their efficiency. This thesis starts with an introduction to millimeter-wave transmitters in CMOS, standards and beamforming. It then continues with a brief introduction to millimeter-wave power amplifier design and design of local oscillators at millimeter-wave frequencies. The last part of the thesis consist of six papers, which present eleven manufactured and measured millimeter-wave circuit designs. Paper I presents a two-stage, 65-nm CMOS, Class-A PA for the 60-GHz band. It employs capacitive cross-coupling neutralization for higher differential isolation and gain, without the need to increase the power consumption. It achieves 18.5 % peak-added-efficiency. Paper II presents a varactorless VCO in 65 nm CMOS, operating in the 60-GHz band. In paper III, the efficiency of the popular source-node filtering technique for improved phase-noise performance is investigated through measurements of two same-chip 60-GHz VCOs in FD-SOI CMOS. The filtered VCO achieves a state-of-the-art figure-of-merit of -187.3 dBc/Hz. Paper IV presents two FD-SOI CMOS VCOs for the 30-GHz and the 60-GHz band, that achieve ultra-low power consumption, also at full supply voltage. In paper V, a phase-locked loop in 28-nm FD-SOI CMOS for 5G transceiver systems is proposed. Its VCO operates at around 55 GHz. The paper describes the disadvantages of using a too high input reference frequency, but also proposes a new architecture that handles the increased settling time by mode-switching. It also includes a novel charge-pump current-mismatch mitigation technique based on feedback, and a novel wideband and low-power injection-locked divide-by-three circuit. The phase-locked loop consumes only 10 mW of power, has an integrated jitter of 176 fs, and demonstrates a state-of-the-art figure-of-merit of -245 dB. Paper VI describes a wideband injection-locked divide-by-two circuit in 28-nm FD-SOI CMOS. It achieves a locking range of 30 % at the low power consumption of 4.3 mW.

Populärvetenskaplig sammanfattning

Vi lever i en uppkopplad värld, där vi tar för givet att det alltid finns mobil- eller WiFi-täckning så att vi kan kontakta dem som vi bryr oss om, hitta rätt i en ny stad, finna nog med information att fatta ett beslut, eller helt enkelt bara roa oss. Detta är inte på något vis endast ett svenskt fenomen. Det finns idag 7,9 miljarder mobilabonnemang på jorden, vilket är 200 miljoner fler än vad det finns människor. En framtidsvision som redan håller på att hända är att inte bara människor, utan även föremål som t ex hushållsapparater, bilar och medicinska implantat skall kunna vara uppkopplade. I varje uppkopplad pryl finns det en sändare och mottagare, som kan omvandla de elektromagnetiska signalerna i luften till digitala data som vi har i våra datorer och telefoner. Eftersom signalerna i luften är analoga, så är även den del av sändaren och mottagaren som sitter närmast antennen analog. Just denna del, specifikt sändaren och dess ingående delar, är vad denna avhandling handlar om. För att en sändare skall passa i konsumentelektronik, måste den vara billig och dessutom strömsnål, så att batteriet håller länge. Billigare kan den bli om man gör den i en vanlig sorts kiselteknologi som kallas CMOS, och strömsnålare kan den bli om man noggrant går igenom varje liten del i sändaren och försöker att hitta nya sätt att spara ström. Sändare utsätts också hela tiden för hårdare krav. Ju bättre upplösning som filmen som vi vill streama har, desto mer data måste vi skicka samtidigt. När alla vill ha högre datahastigheter, tar utrymmet i luften som vi delar helt enkelt slut. Tänk dig ett rum, där alla skriker samtidigt. Ingen kommer att bli hörd och förstådd. Det finns redan många system för att utnyttja vårt gemensamma utrymme bättre, och det finns hårda krav på hur sändare får lov att sända för att störa andra så lite som möjligt. Ett system för att använda rummet bättre, är att alla pratar endast när det är deras tur. Ett annat snillrikt system efterliknar en situation där alla i rummet talar olika språk, vilket gör det lättare att urskilja en enskild person. Ibland använder avancerade system även trattar (antenner) för att se till att ljudet går mest i den riktning som man vill. Att alla pratar på olika frekvenser är ytterligare ett sätt, ungefär som om någon bara får tala med basröst, och någon annan bara i falsett. Men oavsett hur många finurliga sätt som man har kommit på, börjar platsen ta slut. Vad som ligger härnäst i utvecklingen är att tillåta och möjliggöra att kommunikationen kan ske på högre och högre frekvenser. Det är svårt, eftersom naturen har ordnat det så, att ju högre frekvenser som används, desto mer dämpas signalen i luften. Dessutom blir det svårare att använda den billiga och vanliga CMOS-kiselteknologin, eftersom de individuella transistorerna får svårare att hänga med och fungera korrekt. Vad sändarna som den här avhandlingen handlar om måste klara är att skicka rätt data med

en bärvågsfrekvens på upptill ungefär 65 GHz. Eftersom en elektromagnetisk signal med en frekvens mellan 30 och 300 GHz har en våglängd som är mellan en och tio millimeter, så kallas det här frekvensområdet för millimetervågor. Som en jämförelse använder inga mobiltelefoner i dagsläget frekvenser över 6 GHz. Det finns redan produkter som kan kommunicera kring 60 GHz, men jämfört med flera miljarder mobiltelefoner är de är extremt få, och för att kunna bli en del av vår vardag behöver de bli billigare, och förbättras genom att varje individuell del görs mer effektiv. Vi kallar kretsar för mer effektiva om de kan utföra sina uppgifter korrekt men med mindre förbrukad effekt, eller om de kan göra sin uppgift bättre med samma effektförbrukning som innan. Denna avhandling fokuserar på två delar av analoga millimetervågssändare: effektförstärkare, som ofta förbrukar mer än hälften av den totala effekten i en sändare och där varje uns av förbättring ger stora effekter, samt den grupp av kretsar som är ansvariga för frekvensgenereringen. En förstärkare som är ovanligt effektiv i sin klass har konstruerats, likaså en faslåst loop som utför sin uppgift lika bra som andra publicerade faslåsta loopar, men med mindre än halva effektförbrukningen. Olika förslag på ytterligare förbättringar av viktiga delar i faslåsta loopar har utvecklats, och lett till konstruerade och mätta spänningsstyrda oscillatorer och injektionslåsta delare som visar att dessa kretsar kan klara sin uppgift och samtidigt bara förbruka en femtedel till en tredjedel av vad som är standard. Sammantaget presenteras elva kretsar som alla innehåller exempel på hur millimetervågssändare kan bli mer effektiva.

Preface

This dissertation summarizes my academic work for a PhD degree in Electrical Engineering in the Analog RF Design group, at the Department of Electrical and Information Technology, Lund University, Sweden. This work was funded by the Swedish Research Council (Vetenskapsrådet) and the European Commission in the framework of the H2020-ICT-2014-2 project Flex5Gware (Grant agreement no. 671563). The chip fabrication was donated by STMicroelectronics. The dissertation is divided into two parts. The first part gives an introduction to the research field, and the second part consists of the included research papers, as listed below.

Included Research Papers

The main scientific contribution is derived from the following publications:

Paper I T. Forsberg, H. Sjöland and M. Törmänen, "A two-stage mm-wave PA with 18.5% PAE in 65 nm CMOS," in *Proc. of 2015 Asia-Pacific Microwave Conference (APMC)*, Nanjing, China, Dec. 6–9 2015, pp. 1–3. [1]

Paper II T. Forsberg, H. Sjöland and M. Törmänen, "A 65 nm CMOS varactorless mm-wave VCO," in *Proc. of 2014 International Symposium on Integrated Circuits (ISIC)*, Singapore, Dec. 10–12 2014, pp. 54–57.

Paper III T. Forsberg, J. Wernehag, A. Nejdel, H. Sjöland and M. Törmänen, "Two mm-Wave VCOs in 28-nm UTBB FD-SOI CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 5, pp. 509–511, May 2017.

Paper IV T. Forsberg, J. Wernehag, H. Sjöland and M. Törmänen, "Two Ultra-Low Power mm-Wave Push-Pull VCOs in FD-SOI CMOS," in *Proc. of 2018 Asia-Pacific Microwave Conference (APMC)*, Kyoto, Japan, Nov. 6–9 2018, pp. 1–3.

Paper V M. Abdulaziz, T. Forsberg, M. Törmänen and H. Sjöland, "A 10 mW mm-Wave Phase-Locked Loop with Improved Lock Time in 28-nm FD-SOI CMOS," *IEEE Transactions on Microwave Theory and Techniques*, pp 1–12, 2018. *Submitted.*

[1] Won Best Student Paper Award at the conference

Paper VI T. Forsberg, J. Wernehag, H. Sjöland and M. Törmänen, "A 4.3-mW mm-Wave Divide-by-Two Circuit with 30% Locking Range in 28-nm FD-SOI CM," in *Proc. 2018 IEEE Nordic Circuits and Systems Conference (NORCAS)*, Tallinn, Estonia, Oct. 30–31 2018, pp. 1–4.

Related Publications

During my Ph.D. studies, I have also co-authored the following papers, which contain overlapping material, but are not considered a part of this dissertation.

- I. Din, S. Anderson, T. Forsberg and H. Sjöland, "A 24 GHz, 18 dBm, Broadband, Three Stacked Power Amplifier in 28nm FDSOI," in *Proc. of IEEE NORCAS 2018*, Tallinn, Estonia, Oct. 30–31 2018, pp. 1–4.
- A. Bondarik, T. Forsberg, D. Sjöberg, H. Sjöland and M. Törmänen, "Microstrip Antenna Array Integrated with a Two-stage mm-wave CMOS Power Amplifier," *IEEE Microwave and Wireless Components Letters*, 2018. *Submitted.*

Acknowledgments

The work presented in this thesis would not have been possible without the help and support of many.

First of all, I would like to express my sincere thanks to my supervisor Markus Törmänen. One of the most impressive ways that his deep understanding of all subjects at hand manifests is his ability to swiftly find the core of the most complex technical problems and know where to focus to reach a solution. Without his guidance, none of this would have been possible. I will be forever thankful for the chance that I was given to do research in such an interesting field. I am also grateful to my co-supervisor, who is also my initial main supervisor, Henrik Sjöland. Not only is his knowledge of the field brilliant, he has also taught me about how to properly present my research, and he is a true role model when it comes ethical questions surrounding research in general. A huge thank you also goes to my co-supervisor Johan Wernehag, for his support in trying times and his ability to put thing into perspective.

Thank you also to all the people in the Integrated Electronics Systems group that made life in our corridor feel friendly and supportive. I will always remember fondly my fellow PhD students in the RF Analog group that I had the fortune to work with, and that brightened up my days. Thanks to Carl Bryant and Jonas Lindstrand for the circuits that we created once when time was short, thank you to Anders Nejdel and Waqas Ahmad for the collaboration to create pad designs that has since been used by me and many others. I would also like to extend a very special thank you to Mohammed Abdulaziz, who endured long sessions in the lab with me, striving to get our design to work. His untiringly positive outlook on things is truly inspiring and it has set a great example for me.

To all the people at EIT that provide invaluable technical and administrative support: I am grateful for your efforts. Thank you to Göran Jönsson, Andreas Johansson, and Martin Nilsson for maintaining the lab, and to Lars Hedenstjerna for making beautifully perfect parts that made my measurements possible. Thank you to Stefan Molund and Erik Johnsson for not giving up trying to fix all of my software issues. Thank you to Pia Bruhn, Anne Andersson and Elisabeth Nordström for your magical ability to make all my administrative task and questions seem trivial.

During my PhD studies I have been fortunate enough to be able to go to international conferences, through the financial support of ÅForsk, the IEEE Microwave Theory and Techniques Society, and the Royal Physiographic Society of Lund. For this, I am very grateful.

I would like to send a thank you to all the people involved in, and around, the Microwave Electronics Laboratory at Chalmers University of Technology, for allowing me to make some of my measurements with them, and for providing

such a welcoming and scientifically interesting environment.

I owe so much to my previous colleagues at Ericsson in Lund. Sometimes it is Lars Sundström or Peter Caputa that provides me with some invaluable piece of information to further my knowledge, sometimes it is Per Sandrup that helps me to get hold of some crucial software licenses in the middle of Christmas vacations, or Peter Herrder that lends me essential pieces of lab equipment, and always, it is everyone, just being wonderfully supportive.

I would also like to thank my family. To my mother Bodil, my father Bo-Göran, and my mother-in-law Birgitta, thank you for always being there for me. To my amazing sister Ulrika and to Daniel, thank you for being my role models for my academic undertakings, and for being generally awesome people. Thank you to Sven, my kind husband, who has patiently endured my long days before deadlines and never stopped believing in me.

Finally, to all the people that I was unable to mention here, thank you!

List of Acronyms

3GPP	3rd Generation Partnership Project
AM	Amplitude modulation
CML	Current-mode logic
CMOS	Complementary metal-oxide-semiconductor
CP	Charge pump
DAC	Digital-to-analog converter
dc	Direct current
DPD	Digital pre-distortion
FD-SOI	Fully depleted silicon-on-insulator
FOM	Figure of merit
GaAs	Gallium-Arsenide
HBT	Heterojunction bipolar transistor
IF	intermediate frequency
ILFD	Injection-locked frequency divider
ISM	Industrial, scientific and medical
LO	Local oscillator
mm-wave	millimeter-wave
NMOS	n-channel metal-oxide-semiconductor field-effect transistor
NR	New radio
OFDM	Orthogonal frequency-division multiplexing
PA	Power amplifier
PAE	Power-added efficiency
PAPR	Peak-to-average power ratio
PCB	Printed circuit board
PFD	Phase-frequency detector
PLL	Phase-locked loop
PM	Phase modulation
PMOS	p-channel metal-oxide-semiconductor field-effect transistor

PN	Phase noise
PPA	Pre-power amplifier
PSRR	Power supply rejection ratio
QAM	Quadrature amplitude modulation
RF	Radio frequency
SOI	Silicon-on-insulator
UTBB	Ultra-thin body and buried oxide
VCO	Voltage-controlled oscillator
WPAN	Wireless personal area network

List of Symbols

$\&$	Logical AND operation
β	Feedback factor
Δ	Difference
$\Delta\Phi$	Phase difference
Δf	Frequency difference [Hz]
λ	Wavelength [m]
ω	Angular frequency [rad/s]
$\omega_{carrier}$	Angular frequency of the carrier [rad/s]
ω_n	Natural frequency of a PLL [rad/s]
ω_{osc}	Angular frequency of oscillation [rad/s]
ω_{range}	Locking range of an ILFD [rad/s]
ω_{res}	Resonance frequency [rad/s]
ϕ_{in}	Input signal phase
ϕ_{out}	Output signal phase
ω_{res}	Resonance frequency [rad/s]
ζ	Damping factor of a PLL
η	Drain efficiency of a PA [%]
θ	Angle [rad]
A	Amplification, gain
B	Noise integration bandwidth [Hz]
C	Capacitance [F]
C_i	Capacitance i [F]
C_{filter}	Filter capacitance [F]
C_{par}	Parasitic capacitance [F]
C_t	Tank capacitance [F]
CLK	Clock signal
CP_{1dB}	1-dB compression point in a PA [dBm]
DN	The "down"-signal to a CP

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F	Amplifier noise factor
f	Signal frequency [Hz]
f_0	Output frequency of an ILFD [Hz]
f_{bb}	Baseband signal frequency [Hz]
f_{corner}	Flicker noise corner in a VCO [Hz]
f_{fb}	Feedback signal frequency to the PFD in a PLL [Hz]
f_{in}	Input signal frequency [Hz]
f_{LO}	Local oscillator signal frequency [Hz]
f_{max}	Maximum signal frequency [Hz]
f_{min}	Minimum signal frequency [Hz]
f_{osc}	Signal oscillation frequency [Hz]
f_{out}	Output signal frequency [Hz]
f_{ref}	Reference signal frequency [Hz]
f_{res}	Resonance frequency [Hz]
f_T/f_{max}	Frequency of unity current gain/unity power in a transistor [Hz]
G	Gain [dB]
g_m	Transistor transconductance [S]
$H(s)$	Transfer function in the Laplace plane
I	Current [A]
I_{cp}	Charge-pump current [A]
I_{inj}	Injected current [A]
I_{osc}	VCO oscillation current [A]
k	Boltzmann constant $[m^2 \cdot kg \cdot s^{-2} \cdot K^{-1}]$
K_{VCO}	VCO gain [Hz/V]
$\mathscr{L}(\Delta f)$	Single-sided PN [dBc/Hz], at distance Δf Hz from the carrier
L_{filter}	Filter inductance [H]
L_t	Tank inductance [H]
M_i	Transistor i
N	PLL division ratio between output and input signal frequencies

P	Power [W]
P_{dc}	dc power consumption [W]
P_{in}	Input signal power [W]
P_{out}	Output signal power [W]
$P_{out,max}$	Maximum saturated output signal power [W]
Q	Quality factor
R	Resistance [Ω]
R_i	Resistance i [Ω]
R_L	Load resistance [Ω]
r_o	Transistor output resistance [Ω]
R_P	Parallel loss resistance [Ω]
RST	Reset signal
T	Signal cycle time [s]
T_{ref}	Reference signal cycle time [s]
UP	The "up"-signal to a CP
V	Voltage [V]
$V_{b,high}$	dc bias voltage for high-side injection in an ILFD [V]
$V_{b,low}$	dc bias voltage for low-side injection in an ILFD [V]
$V_{b,inj}$	dc bias voltage for high-side injection in an ILFD [V]
V_{bias}	dc bias voltage [V]
v_{ctrl}	Control voltage in to the VCO in a PLL [V]
V_{osc}	Oscillation voltage [V]
V_{in}	Input signal voltage [V]
V_{out}	Output signal voltage [V]
V_{var}	Control voltage to the varactor [V]
V_b	dc bias voltage [V]
VDD	dc voltage supply [V]
X_L	Load impedance [Ω]

Introduction

Chapter 1

Introduction

1.1 Motivation

In today's fast-paced world, we have come to take wireless data access for granted. Wherever we go, we expect cellphone or WiFi coverage to aid us in getting in touch with those important to us, finding our way, acquire enough information to make a decision, or simply to entertain ourselves. The number of cellphone subscribers is steadily rising, and already today there are more than 7.9 billion subscriptions in the world – that is 200 million more subscriptions than there are people [1]. It is expected that in the future, subscribers can also be objects, such as home appliances, cars, or medical implants. Hence, the global mobile data traffic is growing fast, and it is forecasted to keep growing at an even faster pace, as in shown in Fig. 1 [2]. The expected required data speeds are rising along with it. The higher the quality of the photos or movies that we send, the more data needs to be transferred rapidly. This data is modulated onto a signal of a specific carrier frequency when sent though the air, and the wider the frequency span that it spreads over around the carrier frequency, the more data it can carry. But we all share the same air, and if everyone yells at the same time, no one will be heard. Several standards for wireless communication try to solve this problem, restricting when and what each access node can send and employing complex techniques that minimize cross-talk. Soon, however, that will not be enough either. So far, almost all carrier frequencies for wireless communication have been below a few GHz, because wireless communication at higher frequencies is hindered by physical phenomena such as higher in-air attenuation, higher penetration loss, and more shadowing effects from obstructing objects. However, going to higher carrier frequencies for wireless communication is a necessary step in the continuous data revolution. Some future communication frequencies are in the millimeter-wave (mm-wave) range. The name "mm-wave" refers to frequencies between 30 GHz and 300 GHz, where wave-lengths are in the range of 1-10 mm. During the past years, a few systems have demonstrated the feasibility of mm-wave

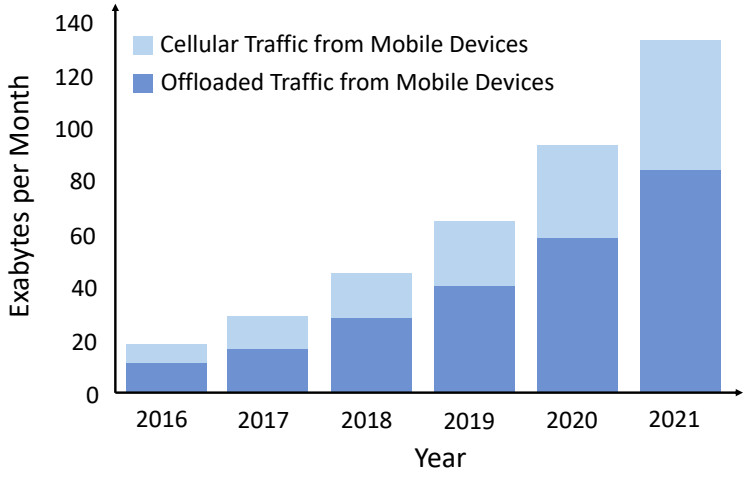


Figure 1: Global mobile data traffic, with forecast. Offloaded traffic is wireless traffic though for instance WiFi or Bluetooth, i.e. not through cellphone networks. Based on [2].

communication, and are today commercially available. However, this does not mean that all problems are solved. To reach a bigger market, the electronics need to be even cheaper. They also need to use less power and still meet the same requirements, which will make batteries last longer and benefits both personal economy and the environment. Going for cheaper circuits often mean using CMOS technology, because it is readily available and adapted for mass-market production. It also facilitates integrating more of the system on the same chip. However, it has some drawbacks compared to other technologies, that need to be addressed and mitigated when designing the transceiver circuits. The cost of manufacturing circuits in CMOS rises with the physical size of the circuit, so they also need to be kept as small as possible. All of these desired traits are interconnected and have complex trade-offs. Some are not entirely understood yet, and all of them are subject to attempts of circumvention.

The aim of this thesis is to investigate how some aspects of mm-wave transmitter circuits in CMOS can be made more efficient, meaning that they are able to perform their task while using both a smaller area and/or a lower power consumption than previous art.

1.2 Outline of the Thesis

The thesis is organized as follows:

Chapter 1 presents the motivation for the dissertation, and its organization.

Chapter 2 introduces mm-wave radio transmitter systems, their building blocks and some commonly used performance metrics.

Chapter 3 explores mm-wave power amplifier design.

Chapter 4 focuses on efficient frequency generation circuits.

Chapter 5 gives summaries and conclusions of the included papers along with the author's contribution.

Chapter 6 provides a discussion with suggestions for future work.

Paper I presents a mm-wave class-A power amplifier with high efficiency.

Paper II presents a varactorless mm-wave voltage controlled oscillator.

Paper III presents an empirical investigation of the impact of using a noise-reducing architecture in mm-wave voltage controlled oscillators.

Paper IV presents two ultra low-power mm-wave voltage controlled oscillators.

Paper V presents a mm-wave analog phase-locked loop for 5G applications, with very low power consumption and an improved lock time.

Paper VI presents a wideband injection-locked divide-by-two circuit.

Chapter 2

mm-Wave Radio Transmitters

This chapter introduces CMOS analog mm-wave transmitter systems. It discusses the environment in which they will work, and presents challenges and solutions related to their design on architecture level.

2.1 Communication at mm-Wave Frequencies

During the past decade, commercial interest in communication on mm-wave frequencies has steadily grown. Expanding to higher frequencies will alleviate the existing congestion in the spectrum below 6 GHz, and at the same time it also promises wider continuous bandwidths and higher data rates. Some frequency ranges in the mm-wave spectrum have attracted special interest, and they will be discussed next. It important to note that since mm-wave communication still has shortcomings, most new standards at mm-wave frequencies are extensions of already existing standards, and their primary use is as a complement to the existing infrastructure.

2.1.1 60 GHz

Around 60 GHz, a worldwide free Industrial, Scientific and Medical (ISM) band offers bandwidths of several GHz. Its allocation depends somewhat on geographical location, as is shown in Fig. 2. One of the reasons to place an ISM band around 60 GHz is because of the increased atmospheric attenuation due to oxygen molecules, see Fig. 3. This means that networks operating on this frequency will by necessity be very local, in practice only within a single room. For a specific sort of networks, this is not a disadvantage, since small networks also mean increased privacy, less interference from other nearby users operating at the same frequency, and a larger potential for frequency reuse.

The first standardized wireless personal-area network (WPAN) in the ISM band to offer Gbit/s data rates is IEEE 802.15.3c, which targets applications such as kiosk downloading, conference ad-hoc systems and video streaming. It divides the band into 4 channels, and each is 2.16 GHz wide [3], as is shown in Fig. 2.

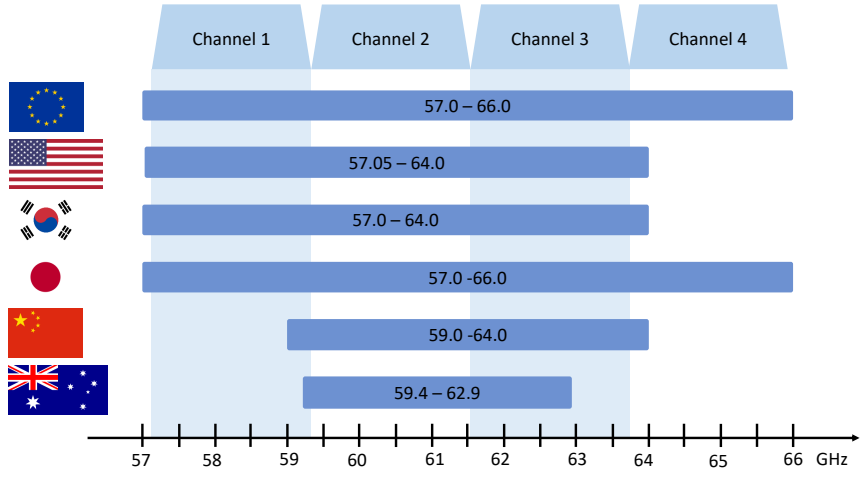


Figure 2: Frequency allocation of the ISM band around 60 GHz, comprised of four subchannels. Based on [3].

The WiFi standard 802.11ad, also known by its previous trade name WiGig, is also implemented in the ISM band. It keeps the proposed division into 4 channels. Although 802.11ad also supports more simple modulation schemes, the primary modulation scheme is orthogonal frequency division multiplexing (OFDM). Using this scheme together with 64-point quadrature amplitude modulation (64QAM), the highest data rates mentioned in the standard reaches 6.75675 Gbit/s, making it one of today's fastest wireless technologies. This puts very stringent requirements on the hardware, and usually also leads to a high power consumption. For this reason, other modes are also available in the standard, that better suits handheld, battery-powered devices. However, all 802.11ad-enabled devices are capable of at least 1 Gbit/s [5].

In the ISM band around 2.5 GHz, new standards have continuously developed over time. Some become very well used, like WiFi and Bluetooth, others become important in niche applications or simply fail to get traction. The same can be expected also for the 60 GHz band. Except for the WPAN and WiFi standards mentioned above, several other standards are already in different stages of development.

2.1.2 70, 80, and 90 GHz

Around 80 GHz, the mm-wave E-band also offers wide bandwidths, without the limitations of high atmospheric attenuation that affects the 60 GHz ISM band. It is, however, more dependent on weather conditions, and the signal will be more attenuated in rainy conditions. The E-band is a licensed band for

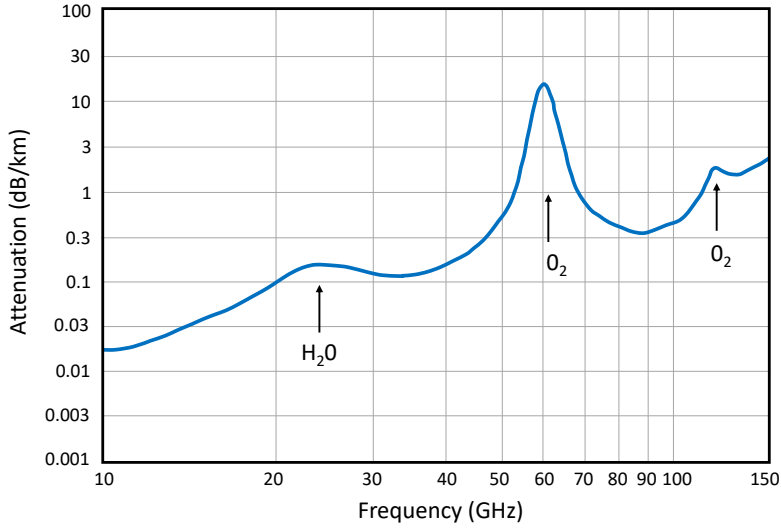


Figure 3: Total attenuation due to atmospheric gases at sea level. Based on [4].

communication, and it consists of three parts of spectrum: 71 to 76 GHz, 81 to 86 GHz, and 92 to 95 GHz. One of its primary planned uses is backhaul for cellular networks. Backhaul is, by definition, a wired or wireless point-to-point communication link. For cellular communication, it denotes the link between a base station and the main switch board. This kind of wireless backhaul in the E-band is especially well suited for the small cells that are anticipated in population-dense areas, where the distance between nodes is no more than about a kilometer [6].

2.1.3 30 GHz

Another of the high-interest frequency ranges is located around 30 GHz. Here, the cellphone industry see a way forward for cellular communication. From the first tentative steps [7], the spectrum around 30 GHz is now becoming integrated into the 3GPP standards, under the name new radio (NR). The planned allocation of spectrum in different parts of the world is shown in Fig. 4, along with the first two named bands. The standard explicitly states that many more bands will be defined within the frequency range in the future. In each band, OFDM will be the primary modulation, and bandwidths up to 400 MHz will be supported [8].

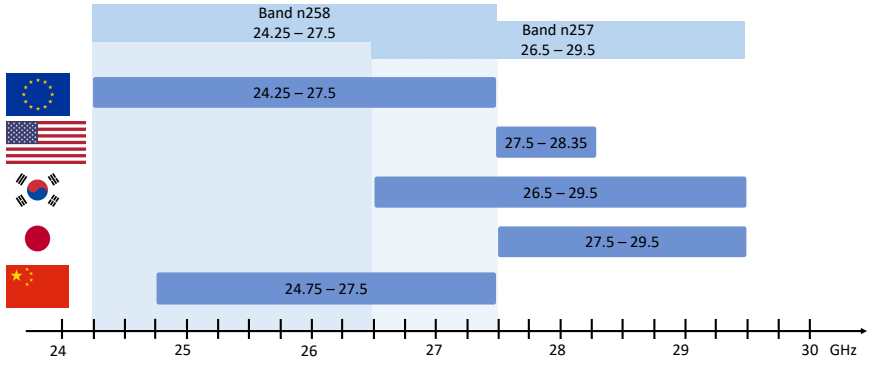


Figure 4: Planned spectrum allocation and band definitions for 5G NR. Based on [8].

2.2 Transmitter Architectures

The basic function of an analog transmitter is summarized in Fig. 5. First, the digital-to-analog converter (DAC) converts the baseband digital signal into an analog one. The analog signal will in practice have some levels of harmonics, noise, and unwanted tones. In each moment, the signal is characterized by its amplitude and phase. Next, mixer(s) upconvert the signal to the target frequency. An ideal mixer multiplies the two input signals in the time domain, and in the frequency domain is creates the sum and difference of the signals. The mixing operation is dependent on the presence of a locally generated frequency signal of good quality. How to create a local oscillator (LO) signal is further discussed in chapter 4. Since the transmitter almost always share a chip with one or more receivers, and they also need an LO signal for their frequency translation, the LO is often also providing signals for the receiver. Finally, in the last step of the transmitter, some amplification of the up-converted signal is needed before it is sent to the antenna. The amplification can be variable or fixed, and it consists of a power amplifier (PA), which is sometimes preceded by a pre-power amplifier (PPA). Power amplifiers are presented in chapter 3. At lower frequencies, filters are usually needed between each stage of the transmitter. However, at mm-wave frequencies, the required filtering can be alleviated, as the individual circuit blocks are tuned to the intended frequency range, providing some filtering.

Generally, transmitter front-ends use either a homodyne or superheterodyne architecture. Both architectures were first described almost a hundred years ago, and both are still commonly used today.

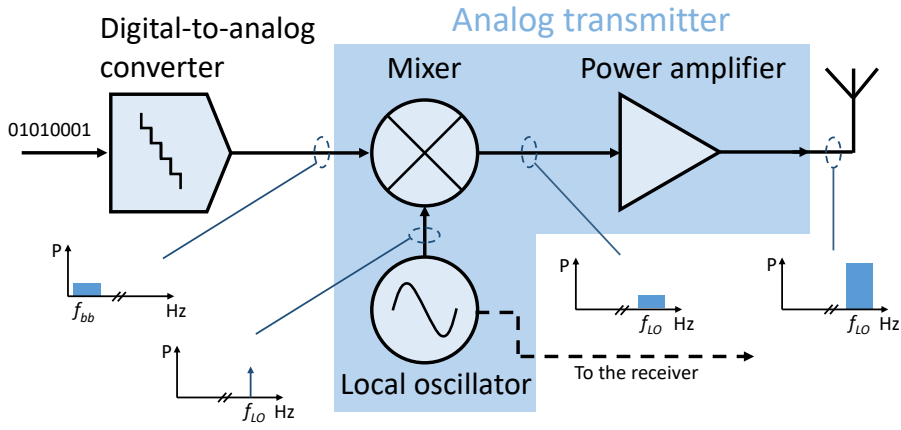


Figure 5: Basic functions of an analog transmitter.

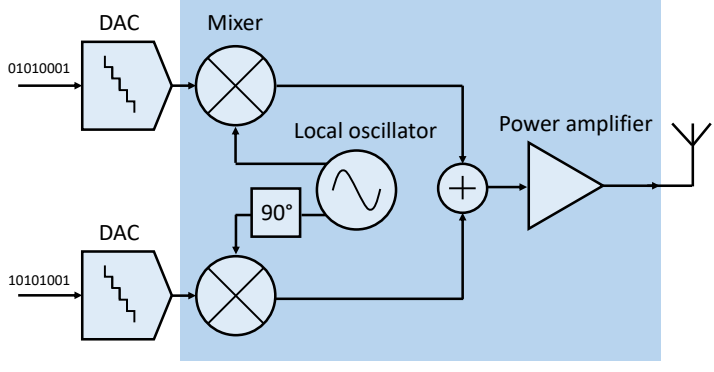


Figure 6: Homodyne transmitter.

2.2.1 The Homodyne Transmitter

The basic principle of a homodyne transmitter is shown in Fig. 6, where I/Q modulation is used. I/Q is short for in-phase and quadrature, and it refers to the practice of using two sinusoidal LO signals that have the same frequency, but are 90° out of phase. Conventionally, the I signal is a cosine waveform, and the Q signal is a sine waveform. This provides a powerful way to create any signal, because any signal can be generalized as

$$x(t) = A(t)cos[\omega_{carrier}t + \phi(t)] \tag{1}$$

$$= A(t)[cos(\omega_{carrier}t)cos(\phi(t)) - sin(\omega_{carrier}t)sin(\phi(t)], \tag{2}$$

where the information is carried by the phase and amplitude. Hence, with the baseband signals defined as

$$x_{baseband,I}(t) = A(t)cos(\phi(t)) \tag{3}$$

$$x_{baseband,Q}(t) = A(t)sin(\phi(t)), \tag{4}$$

it is clear that this architecture can be used to create any signal. For the overall performance of the transmitter, it is very important that the phase difference does not deviate from 90°. An advantage of the homodyne architecture is that it is straightforward, and that it does not require a multitude of subcircuits. However, it demands that all analog parts work at the output frequency, which makes the design more difficult at mm-wave frequencies. The matching between the subcircuits will require more attention, and the local oscillator design will become challenging, especially in terms of noise and balance in the quadrature generation. Also, the PA may disturb and cause pulling in the local oscillator, as it will be working on almost the same frequency.

Some examples of demonstrated homodyne transmitters in CMOS for mm-wave applications can be found in [9–11].

2.2.2 The Superheterodyne Transmitter

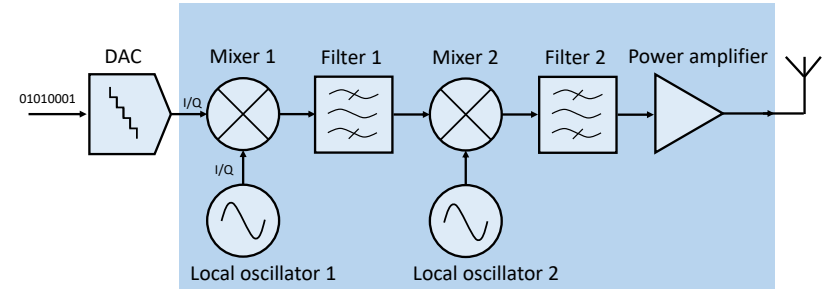
The basic principle of a superheterodyne transmitter is depicted in Fig. 7(a), illustrated as a two-step, single-sideband transmitter. The digital signal is first up-converted to an intermediate frequency (IF), and unwanted signals are removed by a filter. The signal is then upconverted again, using a second mixer and a second LO signal, to the intended carrier frequency.

In practice, the first LO and mixer are often responsible for the quadrature. Since they will operate at lower frequencies than the LO and mixer in the homodyne transmitter, the design will be less challenging. A disadvantage of this architecture is that it introduces additional circuits. However, at mm-wave frequencies, the filters will be less bulky, and the filters can fit on-chip if the IF is chosen carefully. Some recent examples of demonstrated superheterodyne transmitters in CMOS for mm-wave applications can be found in [12–16].

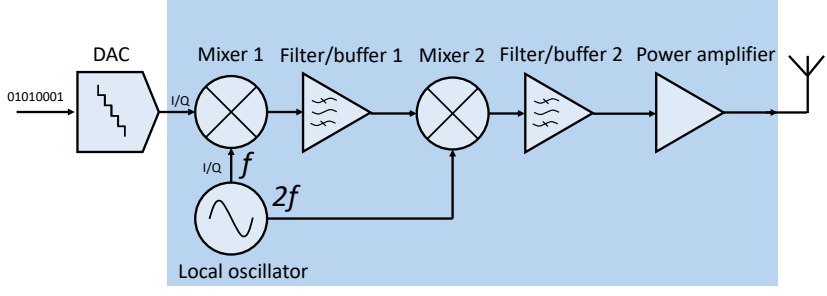
A special case of the superheterodyne transceiver is the sliding-IF architecture. Instead of keeping the IF constant, both LO frequencies move together. One advantage of this is that transmitter may not need multiple LOs. Each LO can be, for example, half of the transmitter carrier frequency, or they can be multiples of each other. Fig. 7(b) shows an architecture that has demonstrated promising results in mm-wave receivers [17].

2.2.3 Transmitter Architectures for Beamforming

Transmission on mm-wave frequencies is, as previously mentioned, difficult due to the high propagation loss. Every obstacle, such as walls or even raindrops,



(a)



(b)

Figure 7: (a) Superheterodyne transmitter. (b) Sliding IF transmitter.

will seem large to the small-wavelength signals. At around 60 GHz the high atmospheric attenuation due to oxygen molecules will add to the attenuation. However, the signal will not only face difficulties going from antenna to antenna. Using CMOS technology for cost and integration benefits will also mean choosing an inferior technology for high-frequency power applications. As technologies are down-scaled, the supply voltage is also scaled down, and the maximum voltage swing the transistors can handle without breaking is also lower. Additionally, the transistor gain decreases with increasing frequency. Hence, it can be difficult to even get a high power output signal to the antenna.

One way to address this problem is to maximize the signal from the antenna by making it increasingly directional, which ensures that all the power arrives at the correct target. Increasing the size of the antenna aperture will increase the directionality of the antenna [18], but also make it a lot more bulky and impractical. To steer the beam in one direction would also require moving the whole antenna. However, an advantage of high frequency communication is that the wavelengths are short and the antennas can thus be small. Instead of

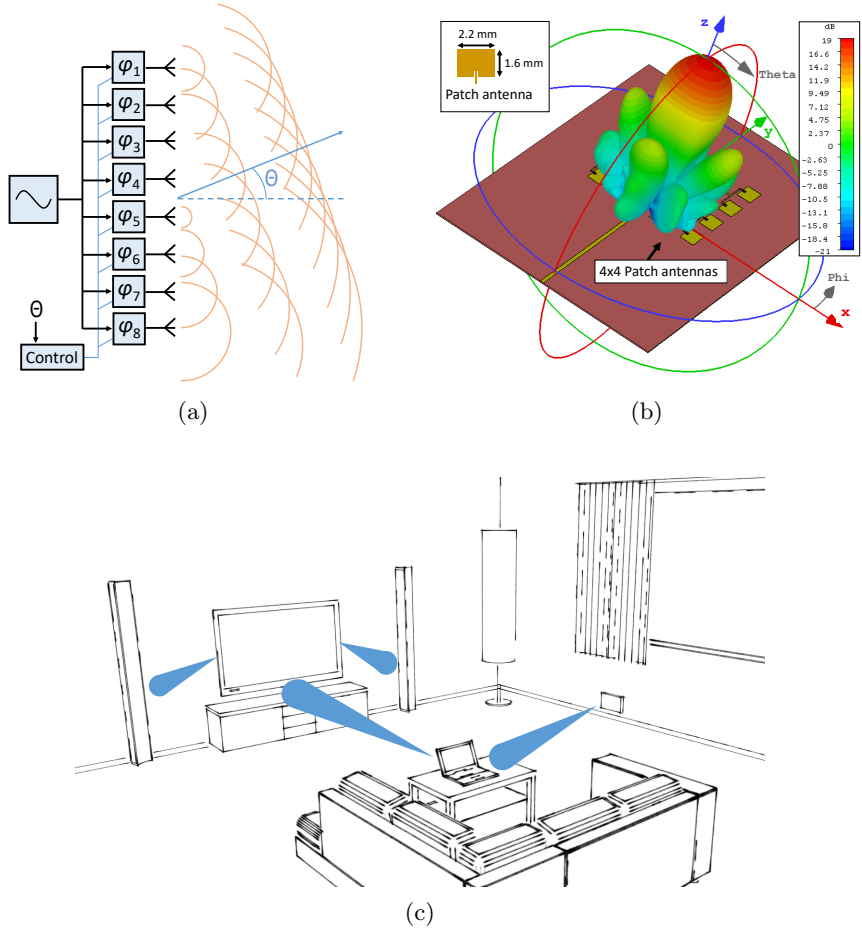
scaling up one antenna, it is possible to use many small, but carefully placed antennas, and make them work together. This configuration is called a phased array of antennas. Even if the signal from each antenna may be weak, many added signals will combine into a stronger signal. By controlling the phase of the signal that is sent from each sub-antenna in the array, they can be forced to create one, directional beam. This technique is called beamforming, and the basic principle is presented in Fig. 8(a). Changing the phase of each signal will quickly shift the beam to point somewhere else, without the need to physically move any antenna. This technique is called beam steering. Figure 8(b) and (c) show examples of this.

To summarize, beamforming and beam steering inherently means using many antennas in an array, and to carefully and continuously control the phase of the signal at each antenna. In practice, also the amplitude to each antenna is controlled, to suppress sidelobes of the signal. The phase shifting circuitry has to be able to produce a wide range of phases, with high resolution and linearity. The phase shift can, in theory, be implemented anywhere in the transmit chain, and each implementation has its advantages and disadvantages.

In one of the extreme cases, the phase shift is performed in the digital domain, and is thus simply called digital beamforming. This requires one DAC and a whole analog transmitter for each antenna. Depending on how challenging the LO signal distribution is, it may be possible to use one LO for all transmitters. In any case, the size of the whole circuit will increase, and the power consumption will drastically increase. However, this solution gives excellent precision, reconfigurability, and spectrum usage due to almost unlimited degrees of freedom.

In the other extreme case, the phase shifters are placed as close to the antenna as possible. The phase-shifting circuits are most often implemented as passive structures, such as delay lines. In this case, only one transmitter is needed for the whole phased array. However, the phase shifting will interfere with the matching between the PA and the antenna, and introduce losses. For these reasons, phase shifting circuitry can be placed before the PA instead. Examples of this can be found in for instance [19], which employs a switched-delay phase shifter, and in [20], which instead has an active vector modulator. The approach to place the phase shift before the power amplifier will create a need for as many PAs as there are antennas in the phased array. However, this suits CMOS PAs very well, since they are less expensive than specialized technologies that have better power-handling capabilities. In any case, when implementing the phase shift at mm-wave frequencies, obtaining enough precision and resolution is difficult. Placing the passive phase shifting circuits in the beginning of a superheterodyne transmitter chain, or simply right after the DAC, will make the control easier, but it will also mean that a larger portion of the transmitter have to be duplicated for each antenna. Another way of creating a phase shift, that does not require passive structures and that has demonstrated the ability

to create a wide range of phase shifts with high resolution, is to perform the phase shift inside the frequency generation circuitry [17].



(a) (b)

(c)

Figure 8: (a) The principle of beamforming, illustrated with a phased array of eight antennas. Each phase shift equals a small time delay of the signal. With the correct timing, the signals from the antennas will create common wavefronts, that move in a defined direction. (b) An example of beam steering. Simulated 60-GHz radiation pattern of a beam and its sidelobes, from a 4x4 phased array of patch antennas on a printed circuit board (PCB). Figure courtesy of Dr. A. Bondarik. (c) An example of how beam steering can be used as a high-speed data wireless interface.

Chapter 3

mm-Wave Power Amplifiers

The PA is the last block in the transmitter before the antenna, and it must be able to deliver the required power to transmit the information, and at the same time meet the requirements on linearity, bandwidth and dc power consumption. This chapter will give an introduction to design considerations for mm-wave power amplifiers (PAs).

So far, the market for hand-held communication devices have favored PAs in technologies like GaAs HBT, that have good power-handling capabilities and work well at high frequencies. CMOS technologies struggle with delivering gain and power at high frequencies, and the limited output voltage swing before the devices break lowers the attainable maximum output power. However, as mentioned in chapter 2.2.3, an individual CMOS transmitter will not necessarily have to deliver as much power if it is used together with other PAs and a phased array of antennas. In that setting, the lower price of CMOS PAs actually makes it preferable. Also, this has huge integration advantages, if the rest of the transmitter is also designed in CMOS technology.

3.1 PA Metrics

The following metrics are the most commonly used metrics to describe a PA.

The **gain** of the PA is the ratio between the average input power P_{in}, in W, and the average output power P_{out}, in W, delivered to the load, i.e. $A = P_{out}/P_{in}$. If all quantities are expressed in decibels, then $G[dB] = P_{out}[dBm]–P_{in}[dBm]$.

When P_{in} is increased, P_{out} will also increase, but only up until the **maximum output power** $P_{out,max}$ is reached. Already before that point, the gain will have decreased. The **1 dB gain compression point** (CP_{1dB}) expresses where the gain has dropped 1 dB compared to the expected value. It is usually related to the output power, in dBm.

Compared to the other parts of a transmitter, the PA consumes a relatively large amount of the total power. Hence, an important metric is the **power consumption** (P_{dc}), and also how efficiently the power is used. The **drain**

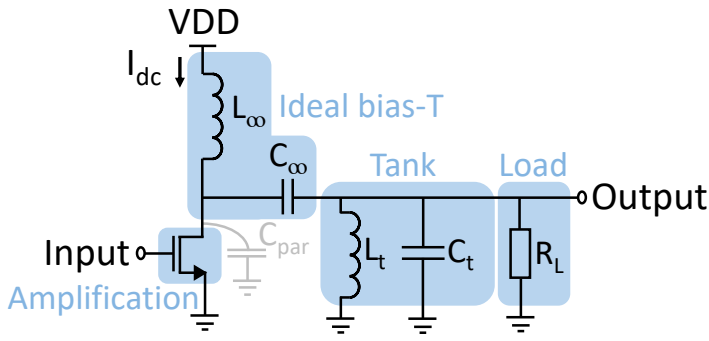


Figure 9: Principle of an ideal tuned PA.

efficiency is defined as $\eta = P_{out}/P_{dc}$. However, since it does not include the input signal power, another metric called the **power-added efficiency** (PAE) is often used instead. It is defined as $PAE = (P_{out} - P_{in})/P_{dc}$.

Since mm-wave PAs are tuned circuits their wideband operation, i.e. their **tuning range**, is also considered.

3.2 PA Fundamentals

An idealized representation of a mm-wave PA is shown in Fig. 9. In this example, the amplification is provided by a transistor in a common-source configuration. The transistor is biased through an ideal bias-T, with an infinite inductance towards the voltage supply VDD that only allows dc to pass through, and an infinite capacitance towards the load. Emphasizing the tuned nature of the PA, the load consists of the explicit load resistance R_L, but also a capacitance and an inductance that in this case forms a parallel resonant tank. The parasitic capacitances of the transistor, C_{par}, will be included in C_t, and likewise, R_L will include the resistive loss in the tank. The resonance frequency of the output circuitry is $f_{res} = 1/(2\pi L_t C_t)$.

3.2.1 Output Matching

As an example, if the aim is to deliver 20 dBm of output power to a 50 Ω load, which is a typical antenna impedance, it will lead to a peak output voltage that is over 3 V. Since this will risk breaking the transistor, an impedance matching network will be placed between the PA and the antenna, to make R_L look smaller when seen from the PA. An example of this is shown in Fig. 10(a) and (b). When transforming R_L in this way, the high output voltage becomes a high output current instead, but the delivered power stays the same. Consequently, the PA transistor must be able to handle large currents to deliver the necessary

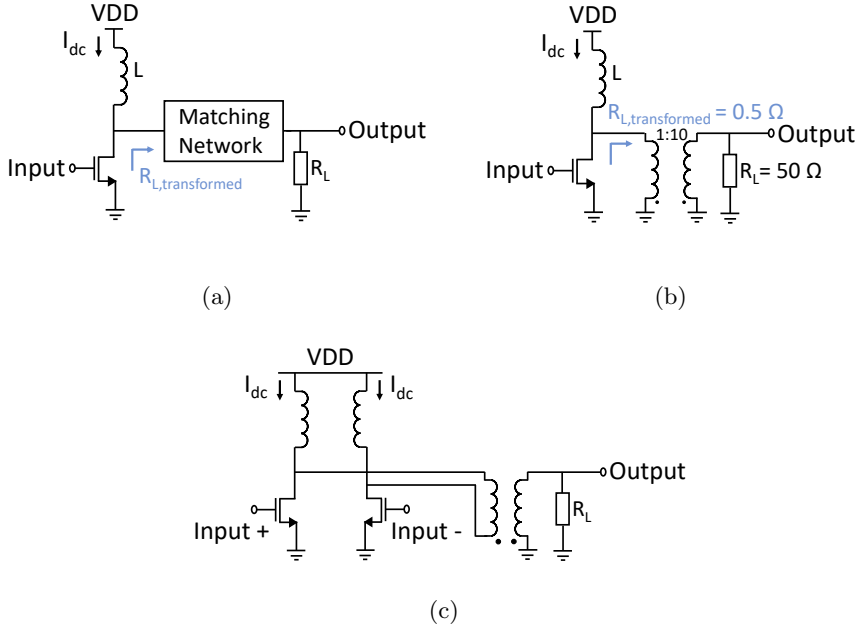


Figure 10: (a) PA with output matching network. (b) PA with a transformer. (c) Differential PA with a balun.

output power. To be capable of that, the transistor size has to be large, and that in turn leads to a high input capacitance. To prevent the high input capacitance from excessively loading the previous stage, i.e. the mixer, PAs are often built with cascaded stages with increasingly large transistors in each stage.

Another reason for the importance of the output matching network is that it plays a role in terminating unwanted harmonics, but at the same time it must have a wide enough bandwidth for the signal. The matching network will be a part of the tank and set the resonance frequency of the PA. When designing a mm-wave amplifier, a design goal for the matching network is to provide the load impedance that maximizes the output power, called power matching or large signal matching. Off-chip matching networks and baluns for single-ended to differential conversion are usually feasible at lower frequencies where packaging capacitances are small. However, at mm-wave frequencies, baluns and inter-stage matching between cascaded PA stages are naturally designed on-chip. Figure 10(c) shows a differential PA with a balun on the output.

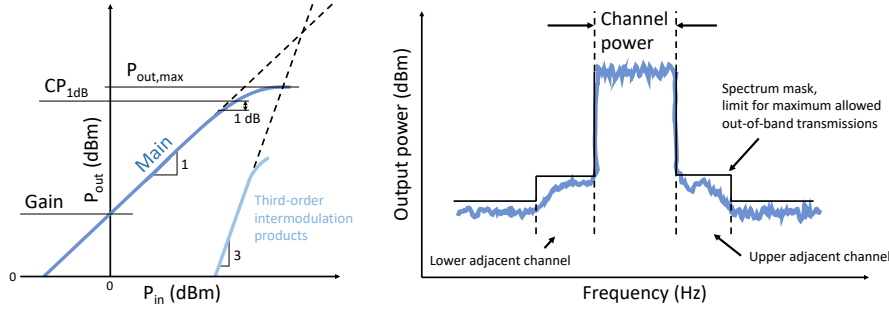


Figure 11: Effects of PA nonlinearities. (a) Relation between input power and output power, and the power in the unwanted third-order intermodulation product. (b) A modulated signal with adjacent channel leakage.

3.2.2 Differential PAs

One of the necessary initial design choices for a PA is whether to use a differential or a single-ended PA topology. Both have advantages and disadvantages. A single-ended PA can be more straight-forward to design. However, the mixer in a transmitter usually has a differential output signal, which benefits a differential PA, but a balun is still needed at the PA output for differential-to-single-ended signal conversion to interface the antenna. Physically, the balun may not consume so much more space, because it can double as a part of the output matching network, as shown in Fig. 10(c). A drawback is that passive components in the transmit chain result in increased signal losses. Other advantages of the differential approach are reduced even-order harmonics, increased dynamic range and less coupling to the LO path.

3.3 PA Classes

Two parameters in PAs are especially dependent on each other, namely the efficiency and the linearity.

The efficiency of a PA is very important, because the PA itself can easily consume more power than all other transmitter parts combined. As an example, if a PA with 50 % drain efficiency has to deliver 30 dBm of power (1 W), it will consume 2 W. The efficiency of a PA will also decrease with input power for almost all PA topologies, and it is rare for any PA to work at its maximum output power for longer periods. Usually, it is working with signals at least a few dBs below their maximum capacity, because modern modulation schemes have high peak-to-average power ratios (PAPR).

Linearity is of concern because it can lead to amplitude compression and

spectral regrowth, which in turn lead to high adjacent channel leakage, see Fig. 11(a) and (b), respectively. Any PA is inevitably nonlinear, since they operate with large signals, but the nonlinearity can be more or less severe, depending on design choices. More complex signal modulation schemes will lead to higher linearity requirements. To estimate the linearity, CP_{1dB} can be measured with a single-tone input, and the intermodulation products can be measured using two input tones. Other nonlinear effects are for instance AM/AM and AM/PM conversion, which is when input amplitude changes create gain and phase variations.

The trade-off between efficiency and linearity is made visible by categorizing PAs into different classes. The most established classes are A, AB, B, C, D, E, F, and inverse F. Generally, the more linear the class is, the less efficient it is. Roughly, the classes fall into two categories: PAs in which the transistor works as a voltage-controlled current source (A to C), and PAs in which the transistor works as a switch (D to inverse F). In the first category, an input sinusoidal signal will, more or less, look like an amplified version of itself at the output. In the second category, the output signal will have lost basically all information that was contained in the amplitude. A very powerful way to correct nonlinearities in PAs is to use digital predistortion (DPD) of the signal. This method uses knowledge obtained though PA calibration to preshape the signal in the digital domain, in a way that counteracts the nonlinearities of the PA. However, DPD may consume a significant amount of power and has its limits. Hence, it cannot always be relied upon to fix the shortcomings of the analog designs.

3.3.1 Class-A PAs

Class-A PAs are among the most straight-forward to design. A PA in class A has a very linear operation, but also the lowest maximum efficiency. However, sometimes the transmitter requires high linearity, which makes class A a good choice despite its low efficiency. Fig. 12 shows class A operation. To ensure that the output signal is always amplified as linearly as possible, the transistors in a class-A amplifier are always on. Since they conduct during the whole period of the sinusoidal input signal, their conduction angle is 360°. The highest efficiency that can possibly be attained is when the output signal is at its maximum voltage swing. However, the maximum drain efficiency will not be reached in real amplifiers, for a number of reasons. The large signals will change the transconductance of the transistors over the period of the signal, and forcing the amplifier to work with too high output voltage while also pushing high currents may cause long-term damage to the circuit. Additionally, the output matching network will add loss, making the maximum theoretical drain efficiency a less realistic goal.

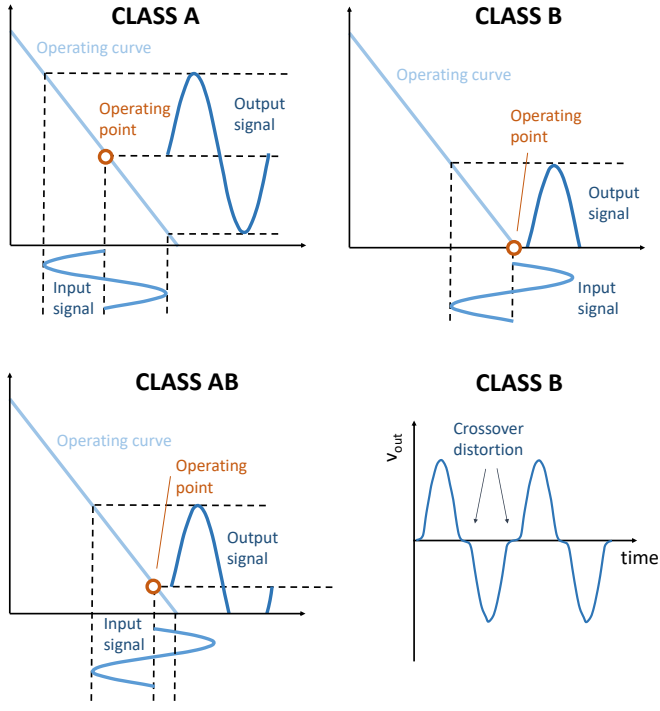


Figure 12: Drain current versus drain-source voltage in class-A, class-B, and class-AB operation. Crossover distortion in class B operation.

3.3.2 Class-AB PAs

The term class-AB is slightly ambiguous. While a class-A PA is linear and has a conduction angle of 360°, a class B PA has a conduction angle of 180°. Traditionally, it is consists of two transistors that work in parallel, and each one is only conducting half of the time. This is achieved by biasing the transistor so that it is not on during the full period. The output will still be quite linear, but suffer from distortion in the transition period, where the voltage is close enough to zero to prevent conduction in any of the transistors. Class B operation is shown in Fig. 12, along with class AB operation. Class AB is just a way of expressing that the PA has a conduction angle between 180° and 360°. It has been demonstrated that advanced CMOS processes are now fast enough to allow mm-wave class AB CMOS PAs that can provide enough linearity for the complex modulations used in the 60 GHz band [16, 21].

3.4 Techniques for mm-Wave PA Efficiency Enhancement

Since the design of the class-A PA presented in this thesis, techniques for enhancing the efficiency in mm-wave PAs have demonstrated increasing maturity. Some examples are given below.

Pushing into deep class AB operation is one way of increasing the efficiency, which have demonstrated good overall performance also at mm-wave frequencies. Except for the negative impact on linearity, it may also cause the power gain to drop. However, an attractive way of increasing the gain and stability of a PA is to use capacitive cross-coupling neutralization, which counteracts the gate-drain capacitance [22]. Figure 13 shows capacitive cross-coupling neutralization in a differential PA. Examples of mm-wave PAs in class AB can be found in [16, 21, 23–25].

Another example is outphasing architectures, where the signal is split into two parts before the PA: one contains the phase information of the signal, and the other one contains the amplitude information. The signals are then amplified separately using nonlinear, but efficient switching PAs. Finally, the signals are combined before the antenna. This architecture has attracted a lot of interest [26–28], and challenging design aspect is the implementation of the final combiners, which may introduce loss and distortion.

Progress in efficiency enhancement has also been made by using dual-mode PAs, which can switch between high-power and low-power mode depending on the momentary transmitter need [23, 29–31]. Some also include frequency reconfigurability [32]. They suffer from the same kind of difficulties as the outphasing designs, with challenging output power combiner design and layout floor planning, but demonstrate state-of-the-art performance.

Even Doherty PAs, a topology that has proven invaluable at lower frequencies to battle low efficiencies at power back-off, have been successfully demonstrated in CMOS at mm-wave frequencies, for instance in [33–36]. However, Doherty PAs are difficult to adapt to wideband operation.

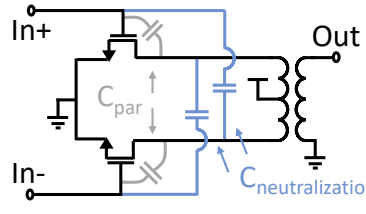


Figure 13: Example of cross-coupling neutralization in a differential PA. The optimal neutralization capacitance matches the parasitic gate-drain capacitance of the transistors.

3.5 Techniques for High Output Power

To obtain high output power from CMOS PAs, one of two paths is typically chosen [37]. The first is to use a high supply voltage and stacked transistors, which is possible without exceeding breakdown voltages if a silicon-on-insulator (SOI) CMOS technology is used [38, 39]. The second is to use passive power combination networks to add the power from several individual PAs. Although the power combination networks are inevitably lossy and degrade the efficiency, they are capable of achieving high maximum output powers [40–42]. An example of a parallel-series combiner is shown in Fig. 14.

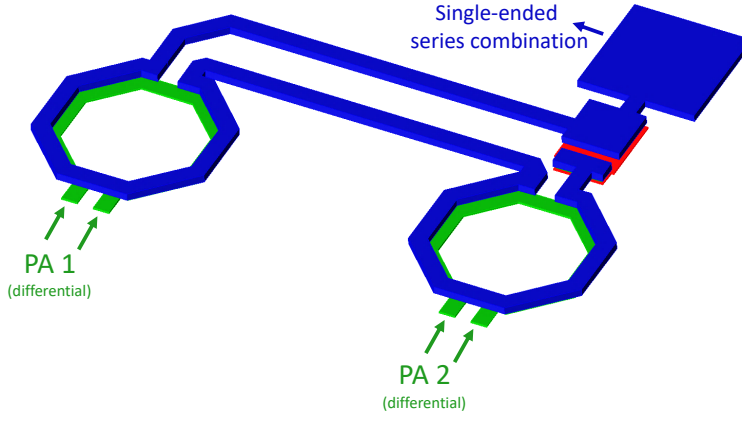


Figure 14: Example of a series power combiner for CMOS PAs.

Chapter 4

mm-Wave Frequency Generation

An integral part of any transceiver is the local oscillator. In a homodyne transceiver design, it provides the carrier frequency signal, onto which the data to be transmitted is modulated. In a superheterodyne transceiver, one local oscillator signal is required for each mixer. In each case, the LO needs to be able to produce a wide range of frequencies with enough output power, and add as little noise as possible to the signal to be transmitted.

This chapter will first discuss voltage-controlled oscillators (VCOs), and then phase-locked loops (PLLs) will be introduced. For both, some common metrics, design challenges, and solutions at mm-wave frequencies will be presented.

4.1 Voltage Controlled Oscillators

An oscillator can generally be described as a highly non-linear circuit that converts dc power into an output ac waveform. The frequency of its output signal is set using a control signal, which is most commonly a voltage. This chapter briefly covers the VCO fundamentals and a closer look at the cross-coupled VCO topology, along with some design considerations and examples.

4.1.1 VCO Metrics

When designing a VCO for a transceiver system, the most common design considerations concern the following properties of the VCO.

The **Frequency range** (Hz) of the VCO declares what frequencies the VCO can synthesize. Unless stated otherwise, it is inferred that all frequencies within the range are possible to create. In the middle of the frequency range is the **center frequency** (Hz), which should coincide with the center frequency of the targeted frequency band. The VCO **tuning range** (Hz), is expressed in GHz as f_{max}–f_{min}, or in percent as $100 \cdot 2 \cdot (f_{max} - f_{min})/(f_{max} + f_{min})$. Designing the tuning range so that the VCO covers a wider frequency span than the intended frequency band is needed to account for variations due to process and operation temperature. In practice, some connections between the

two exist. For instance, achieving a higher tuning range is more difficult at a higher center frequency because parasitic capacitances will limit the range of the variable capacitance. Connected to the frequency range is also the VCO gain, defined as output frequency change per control voltage change (Hz/V). A high gain makes it possible to cover a wide tuning range, but may also be problematic if the VCO gets too sensitive to small variations, i.e. noise, on the control voltage. The ideal frequency vs control voltage function within the frequency range is a straight line with a constant gain, but in practice the gain often varies. For instance, if an NMOS varactor is used for the frequency tuning, the result will be an S-shaped curve with less gain close to the minimum and maximum input control voltage.

Depending on the intended use of the VCO, some **output requirements on waveform, power, voltage swing and drive capability** must be met. The VCO will drive mainly capacitive loads, such as mixers, dividers or buffer amplifiers. Generally, the loss in a passive mixer will be less, the higher the input voltage swing from the VCO is. In an ideal case, the VCO output would be a square wave that switches as abruptly as possible. In practice, the output will be more of sinusoidal shape because the higher harmonics will be filtered out by the relatively narrow-band VCO.

The **Phase noise** (PN) of the VCO profoundly affects the performance of the whole transceiver circuit. The phase noise metric describes how much the frequency of the VCO signal statistically deviates from the intended frequency. In practice, all VCOs will exhibit this kind of noise, and it has trade-offs with both the tuning range and the power consumption. The phase noise is measured in dBc/Hz at some offset from the VCO oscillation frequency, often expressed as $\mathscr{L}(\Delta f)$.

The **power consumption** (P_{dc}), in W, of a VCO is always important, especially if the VCO is to be a part of hand-held battery-powered devices. It is also an important parameter to consider, as both the phase noise and the tuning range can be directly improved by increasing the power consumption.

The VCO may also be more or less sensitive to unintended inputs from its surrounding environment. **Pushing** and **power supply rejection ratio** (PSRR) concerns the sensitivity to changes in the supply voltage, like a voltage drop or supply voltage noise. **Pulling** is when the VCO frequency is changing with the load impedance.

The VCO **figure-of-merit** (FOM) combines some of the most important metrics above into one number, to facilitate comparison between different VCO designs. To assign fair weights to the different parameters, the most used FOM is built upon the heuristic Leeson model of phase noise in oscillators [43], where known trade-offs in VCO design are established. This FOM has unit dBc/Hz and it is calculated as

$$FOM = \mathscr{L}(\Delta f) - 20log(f_{osc}/\Delta f) + 10log(P_{dc}/1mW), \tag{5}$$

where $\mathscr{L}(\Delta f)$ is the the phase noise in dBc/Hz, measured at distance Δf Hz from the carrier oscillation frequency f_{osc} in Hz, and P_{dc} is the power consumption in W. Obviously, a FOM will always be general as it does not take into account the specific requirements of individual applications.

4.1.2 VCO Fundamentals

The simplest model of a basic VCO is a linear feedback model, as shown in Fig. 15. Considering only the dependence of frequency in the amplification $A(\omega)$ and the feedback path $\beta(\omega)$, the relation between input and output voltage can be expressed as

$$V_{out} = \frac{A(\omega)}{(1 - (A(\omega) \cdot \beta(\omega)))} V_{in} \tag{6}$$

When some frequency ω_{res} makes the denominator of Eq. (6) equal to 0, the gain will also be infinite, and an oscillation will spontaneously start. An oscillation can also start at all frequencies within the 3-dB frequency bandwidth of the circuit, provided that it is initiated by the ever-present device noise. However, as the oscillation amplitude increases and eventually stabilizes at some amplitude, both the amplification and the feedback in the system also become dependent on the oscillation amplitude V_{osc}. The criteria for oscillation will then instead become $|\beta(\omega_{osc})A(0)| > 1$ and $|\beta(\omega_{osc})A(V_{osc})| = 1$ and $\angle(\beta(\omega_{osc})A(V_{osc})) = 360°$. In other words, the gain around the loop exceeds 1 at startup, and the oscillation is sustained when the phase around the loop is 360° and the gain around the loop is 1.

4.1.3 The Cross-Coupled Oscillator

A very commonly used architecture for CMOS VCOs, appreciated for its versatility and ease-of-use, is the cross-coupled design. One of its most basic forms is shown in Fig. 16, but countless variations of its basic structure exist. This

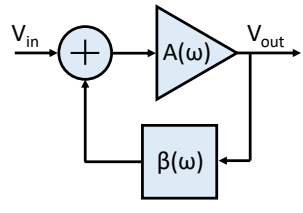


Figure 15: A linear feedback model of a VCO.

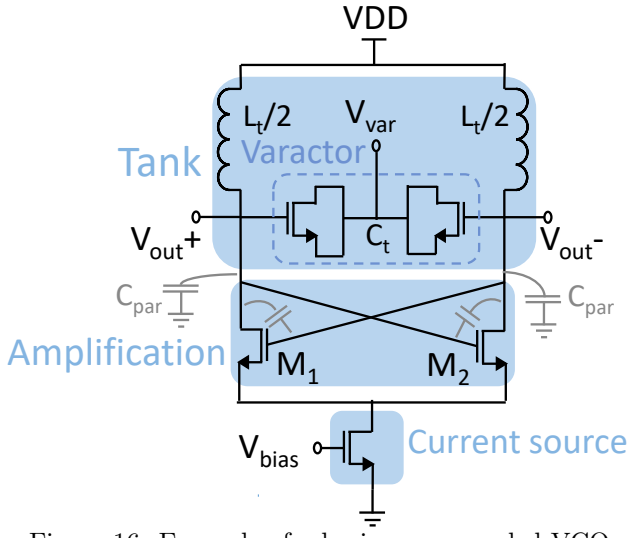


Figure 16: Example of a basic cross-coupled VCO.

VCO generates a differential output signal, taken from the drain terminals of the NMOS devices M_1 and M_2. The signal in the example figure will be sinusoidal, with some harmonic content. The signal will ideally swing around VDD, with a swing of VDD.

The self-oscillation frequency is set by the tank, which consists of an inductance L_t and a capacitance C_t. Both of these circuit elements will also contribute to a parallel loss resistance R_P. The loss resistance R_P will also include the output resistance of the transistor, r_o. C_t also includes the parasitic capacitances C_{par}. The self-oscillation frequency will be $f_{osc} = 1/(2\pi\sqrt{L_t C_t})$. To be able to tune the self oscillation frequency, a part of C_t is often made variable, and in the example in Fig. 16, the variable part is a varactor.

At the self-oscillation frequency, the value of the tank impedance will be just R_P. The voltage gain of each common-source stage is then $-g_m R_P$. Hence, the oscillation criterion becomes $g_m R_P > 1$. In practice, g_m is always designed with some margin to account for process and temperature variations. A variable current source at the source nodes of $M1$ and $M2$, as depicted in Fig. 16, provides an additional possibility to adjust g_m. In some applications, however, it is simply omitted to permit more voltage headroom in the circuit.

4.1.4 VCO design for Low Phase Noise

Phase noise is a very central concept in VCO design. It has been extensively researched for many decades [43–46], and new research into the phenomenon still results in new insights [47, 48].

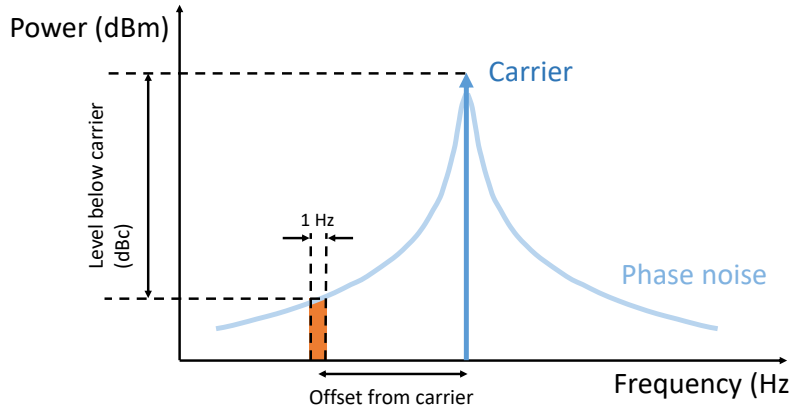


Figure 17: Phase noise.

Ideally, the output of the VCO is a single, stable frequency. If this was the case, the signal that is up- or downconverted with the VCO signal will be a perfect, frequency-translated version of itself, and even closely spaced channels can coexist without interference. However, in reality there will be random phase fluctuations. Intuitively, the signal more often stays close to its intended frequency, and more rarely occurs further away from it. Hence, the output of the VCO has a skirt-like spectrum centered around the oscillation frequency, see Fig. 17. In a transmitter, it will lead to spectral regrowth, and it can make symbols in complex modulation schemes uninterpretable. Since the LO is often also used for the receiver chain, it is worth noting that a receiver is even more vulnerable to LO phase noise.

A complete analytical model of phase noise in oscillators in every silicon technology is very difficult to develop, since the noise is a small perturbation of a large signal present at the transistors, and hence small-signal approximations can not be used. Even if the noise cannot be expressed in an analytical model, measurements and modern simulation tools can still be used to predict and understand phase noise. Already in 1966, Leeson formulated a simple model that describes phase noise in LC feedback oscillators [43]:

$$\mathscr{L}(\Delta f) = 10log\left[\frac{FkTB}{2P_{carrier}}\left(1+\left(\frac{f_{osc}}{2Q\Delta f}\right)^2\right)\left(1+\frac{f_{corner}}{\Delta f}\right)\right] \qquad (7)$$

where $\mathscr{L}(\Delta f)$ is the single-sided phase noise at distance Δf Hz from the carrier, F is the amplifier noise factor, k is the Boltzmann constant, T is the temperature in Kelvin, B is the bandwidth of integration for the noise (typically set to 1 Hz), f_{osc} is the frequency of oscillation in Hz, Q is the quality

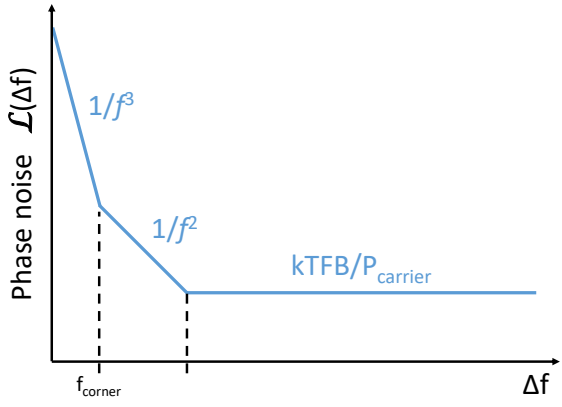
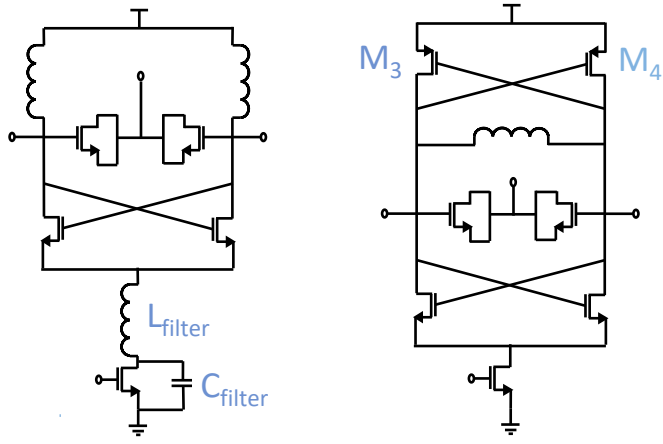


Figure 18: Phase noise regions.

factor of the tank, and f_{corner} is the flicker noise corner. To summarize, there are three distinguishable regions of the phase noise behaviour, see Fig. 18. Far from the carrier, the phase noise will be effectively white. Closer to the carrier, inside the bandwidth set by the Q of the tank, the phase noise will increase as $1/f^2$, i.e. 20 dB/decade. In the region closest to the carrier, the flicker noise will be dominant, and the phase noise will increase as $1/f^3$. Most often, the regions closest to the carrier are the ones of interest, and for VCOs, the noise at 1 or 10 MHz offset from the carrier is often quoted. The frequency that separates the $1/f^2$ and $1/f^3$ regions is called the flicker noise corner.

From Eq. 7, it can be concluded that the most influential contributor to phase noise is the Q value of the tank, and the lower the value, the higher the phase noise. Hence, trying to create a more wideband VCO using a tank with a lower Q-value results in high phase noise. Also, the VCO voltage swing should be maximized to reduce phase noise, but still stay within safe operation limits of the transistors. The noise from each individual transistor should also be kept as low as possible, as should the noise originating from outside sources. Among these are noise from buffers, on the supply voltage or on the control voltage input. The amplitude limitation mechanism of the VCO also plays a part, as the noise performance will be degraded when the transistors stay in triode for too long during each cycle. The phase noise performance will be optimized when the resonance tank is on the verge of being current limited. As identified in [49], the NMOS transistor in the tail current source will spend most of its time in triode, meaning that the current will not stay constant, and neither will the drain current of the cross-coupled transistors. Effectively, the VCO will sample the noise at twice the oscillation frequency when the differential voltage is zero, and actually half the noise from the current source lie around frequencies



(a) (b)

Figure 19: Basic VCO variations. (a) A low phase noise VCO with current source filtering. (b) A push-pull VCO for low power consumption.

close to the second harmonic. To address this, a very useful variation on the cross-coupled topology was presented in [50], see Fig. 19(a). It inserts a filter around the current source, tuned to twice the oscillation frequency. It also introduces a capacitor in parallel with the current source, to provide the noise from the current source transistor with a short path to ground. In practice, it trades area for phase noise, but this also makes it practical at mm-wave frequencies, because of the small geometries at shorter wavelengths.

4.1.5 VCO design for Low Power Consumption

As previously discussed, there is a trade-off between phase noise and power consumption. However, instead of sacrificing the phase noise performance, some other options exist. Several ultra-low power mm-wave VCOs based on the cross-coupled topology have recently been demonstrated [51–53]. One example that achieves low power consumption, by increasing the Q-value of the tank by increasing the size of the inductance and reducing the varactor size, is presented in [51]. As expected, the drawback is a very small tuning range. Many demonstrated ultra low-power VCO designs use lowered supply voltages [52,53],

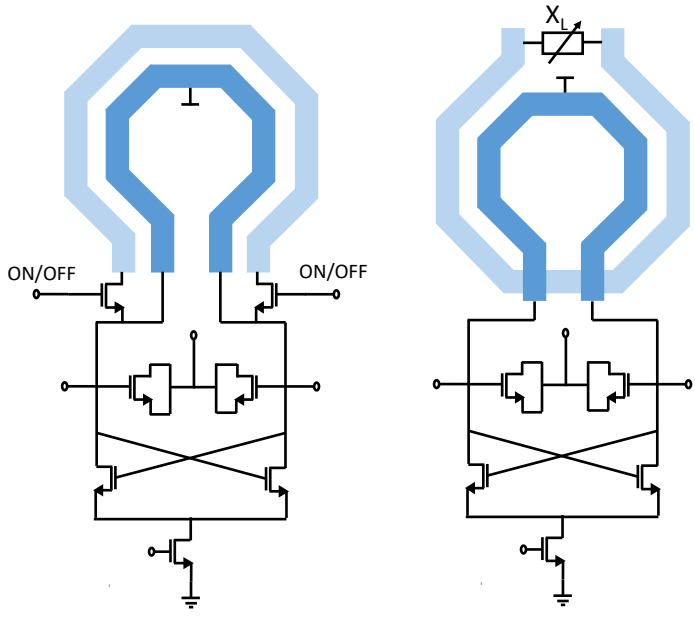
which can lead to excellent power consumption and low phase noise. However, the output voltage swing will be degraded, and a buffer may be required to follow the VCO, ultimately adding to the power consumption. A further drawback if this VCO design is that when put in a transmitter, a separate voltage domain has to be created. Another way to go is to extend the cross-coupled topology with another cross-coupled pair of PMOS transistors. An example of this topology, with PMOS transistor M3 and M4, is shown in Fig. 19(b). As demonstrated in Paper IV in this thesis, it can achieve ultra-low power consumption. One drawback is that the maximum output voltage swing will only be between 0 and VDD, but this can be preferable to ensure long-term stable operation of the VCO.

4.1.6 VCO design for Wide Tuning Range

If no extra measures are taken to expand the tuning range, a CMOS cross-coupled oscillator at 60 GHz with a reasonably sized varactor as the frequency-control mechanism typically has around 10 % tuning range. One reason for this is that varactors usually have low Q values at mm-wave frequencies, and that increasing the tuning range by increasing the varactor size would decrease the parallel resistance in the tank. To compensate for the lower signal swing, the cross-coupled pair transistors have to be larger, which in turn increases their parasitic capacitance, limiting their tuning range and lowering the maximum oscillation frequency.

Even if 10 % would be enough to precisely cover the ISM band in parts of the world, a wider tuning range is needed to ensure that the band is covered, also when variations in process, supply voltage and temperature cause the frequency range to shift. Hence, it is obvious that special measures must be taken to increase the tuning range, and during the past years this has attracted a lot of research interest [54–57].

Some main approaches can be distinguished. One is to circumvent the problem by designing a VCO that is working at lower frequency, and feed its signal to a multiplier, which creates the desired frequency [54]. It facilitates the VCO design, but the noise increases when the signal is upconverted. However, extracting and boosting a harmonic signal directly from a VCO as in [55], has demonstrated good phase noise performance as well. If the parasitic capacitances can be kept small and the Q-value high enough, it is possible to use a VCO directly at the intended mm-wave frequency and use a capacitance bank for the coarse tuning, as is commonly used in VCOs at lower frequencies. An example of this is [56], that employs a capacitor bank and a back-gate controlled varactor. Another solution is to create some coarse tuning by switching in different inductors in the tank, as demonstrated in for example [57]. The concept is presented in Fig. 20(a). The main challenges of these designs are the layout around the extra inductors, and the inevitable extra loss added by



(a) (b)

Figure 20: Basic VCO variations for increased tuning range. (a) A wide tuning range VCO with switched inductances. (b) A wide-band VCO with a transformer.

the switches. In [58] and [59] the effective impedance is tuned by changing the magnetic coupling between different coils, and yet another approach is to make the tank inductance part of a transformer, to be able to change the effective impedances in the tank by switching in different loads through the transformer [60]. An example of this concept is shown in Fig. 20(b).

Most of these methods for extending the tuning range would be compatible with the current-source filtering technique for improving the phase noise performance that is investigated at mm-wave frequencies in this thesis. This could lead to VCOs that are both wide-band and low-noise.

4.2 mm-Wave Phase-Locked Loops

Instead of simply using a VCO as the local oscillator in a tranceiver, it is common practice to instead employ a PLL for the frequency generation. A PLL is a circuit that contains a VCO to synthesize a frequency, but at the same time decreases the VCO phase noise at frequencies close to the carrier. The PLL is

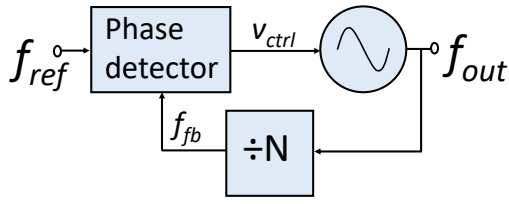


Figure 21: Basic PLL.

able to do this because the control voltage to the VCO will be controlled by a feedback loop that works in the phase domain, and forces the phase noise of the VCO to follow the phase noise of an input reference frequency. Since the reference frequency is generated at a lower frequency, it can be very clean from noise, especially if it is generated with a crystal oscillator. The basic concept of a PLL is shown in Fig. 21. The phase detector will detect any difference in phase between the input reference frequency, f_{ref}, and the divided version of the VCO frequency, f_{fb}. The output of the phase detector, V_{ctrl} will be the control voltage of the VCO.

4.2.1 PLL metrics

The following metrics are the most important in PLL design.

As for the VCOs, the **tuning range**, in GHz or percent, and the **center frequency** in GHz, are important parameters. Naturally, so is the **power consumption**, P_{dc}, in W. Also similar to the VCO, the phase noise, in dBc/Hz, is an important measure. In a PLL, the phase noise will often be presented as integrated over a limited frequency range and related to the output frequency. This is the **integrated average jitter**, called root-mean-square (RMS) jitter, which is measured in seconds. Depending on what PLL topology is used, different levels of unwanted spurs can appear in the output spectrum. Hence, the **output spur levels** in dBc must also be taken into account. Finally, the **lock time**, i.e. the time it takes for the PLL to lock to the desired output frequency in case of a frequency change, is an important parameter. For radars, another way to measure the speed of the PLL is often used, called the **slope**, in Hz/s.

4.2.2 PLL Architectures

The most popular type of PLL, for any application, was for many decades the analog PLL. Recently, subsampling PLLs [61,62], and also all-digital PLLs [63, 64] have made their way also into mm-wave designs and demonstrated excellent performance. However, this thesis will focus on analog PLLs, specifically the

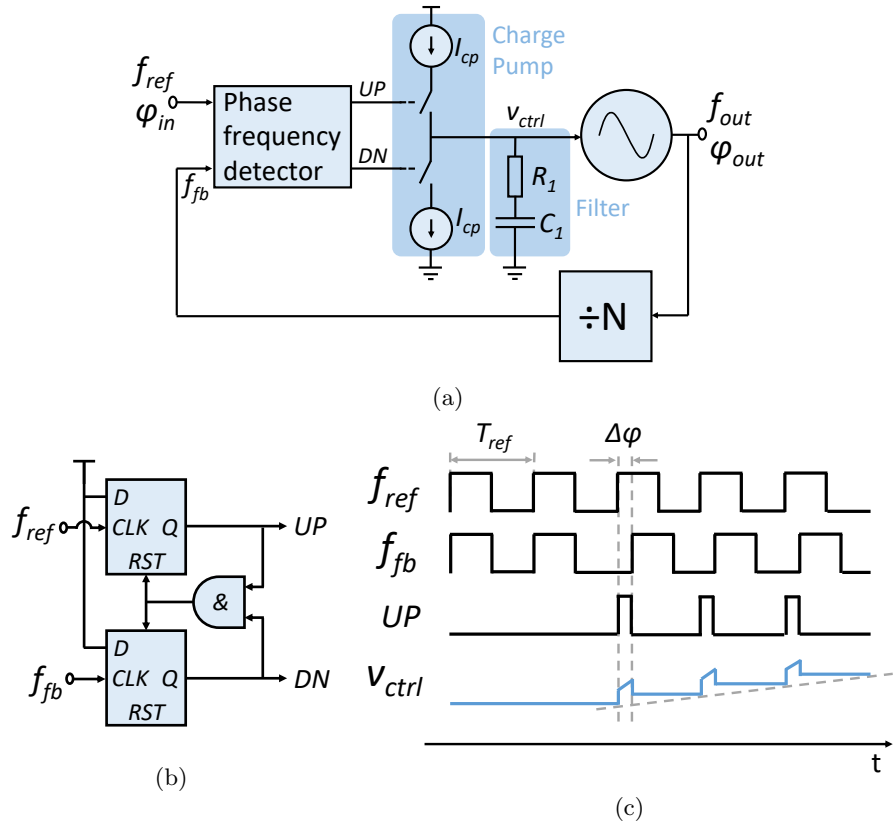


Figure 22: Type-II PLL. (a) Architecture. (b) PFD implementation with D-flipflops. (c) Waveforms in the phase-frequency detector and charge pump.

well-known charge-pump or type-II PLL, and ways to improve its architecture and parts.

Figure 22(a) shows a very common way to implement a PLL. An implementation of a phase-frequency detector (PFD) using resettable, edge-triggered D-flipflops is shown in Fig. 22(b). The PFD reacts to the phase difference on its inputs, se Fig. 22 (c). If the feedback signal arrives later than the reference signal, it will produce an output voltage on the UP terminal, lasting from the rising edge of the reference signal and until the rising edge of the f_{fb} signal. Ideally, it will not produce a DN signal, but in practical implementations there will be a short glitch. The UP signal will turn the upper switch on, and because the DN switch is off, current will flow into the filter capacitor, increasing the voltage in the node V_{ctrl}. This in turn changes the frequency of the VCO, and

if the loop is connected properly, makes the VCO output frequency closer to the correct one. Similarly, if the feedback signal leads the reference signal, the PFD will produce output voltage on the DN signal, and the lower switch will be on, and unload current from the filter capacitor and lower the value of V_{ctrl}.

The closed loop transfer function in the Laplace domain, for small signals, can be expressed as [65]

$$H(s) = \frac{\frac{I_{cp}K_{VCO}}{2\pi C_1}(R_1C_1s+1)}{s^2 + \frac{I_{cp}K_{VCO}}{2\pi N}R_1s + \frac{I_{cp}K_{VCO}}{2\pi C_1 N}} \tag{8}$$

where I_{cp} is the charge pump current, K_{VCO} is the gain of the VCO, R_1 and C_1 are the values of the filter components, and N is the division number in the feedback division chain. The charge-pump PLL has two poles in its transfer function, hence the name type-II PLL. Rewriting the denominator on the form $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ζ is called the damping factor, and ω_n is called the natural frequency, gives

$$\zeta = \frac{R_1}{2}\sqrt{\frac{I_{cp}C_1K_{VCO}}{2\pi N}} \tag{9}$$

$$\omega_n = \sqrt{\frac{I_{cp}K_{VCO}}{2\pi C_1 N}} \tag{10}$$

and that the closed-loop poles are given by $\omega_{p1,2} = [-\zeta \pm \sqrt{\zeta^2 - 1}]\omega_n$. Having established that a PLL is a negative feedback system, and using these equations as a base, it is possible to look into the stability, noise performance, and tradeoffs in the design of a charge-pump PLL.

The PLL will reduce the noise by tying it to the input reference phase noise, but only close to the output frequency, within the bandwidth of the PLL. Here, the phase noise of the free-running VCO will be shaped by the transfer function. However, inside the bandwidth, the reference phase noise in a charge-pump PLL will be scaled up as N^2, and the noise from other circuits in the PLL, such as the charge pump, will be added. Hence, the bandwidth is often chosen to be around the intersection of the free-running VCO phase noise and the reference phase noise, see Fig. 23(a). However, other considerations also apply when deciding the bandwidth of the PLL. For instance, an often-used rule-of-thumb [66] is that the bandwidth should never be more than 1/10 of the reference frequency f_{ref} to ensure that the PLL acts as a continuous-time system. The bandwidth is also linked to the settling time of the PLL, i.e. how fast it will lock to a new frequency if a step is introduced in the loop. For small ratios between f_{ref} and the loop bandwidth, the settling time decreases with increasing bandwidth. However, for high ratios a phenomenon called cycle slips will make the setting time increase again. Figure 23(b) shows the settling behaviour of a PLL with visible cycle-slips. For f_{ref}-to-loop bandwidth ratios of

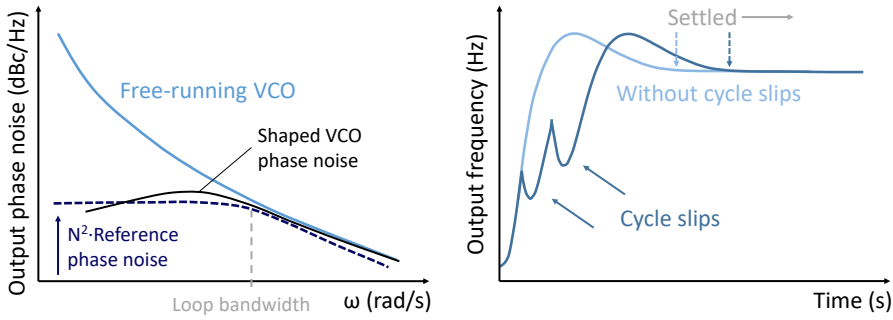


Figure 23: PLL loop dynamics. (a) Noise shaping in a charge-pump PLL. (b) Settling behaviour with and without cycle slips.

a hundred or more, the settling time will be excessively long [67]. Cycle slips are difficult to describe analytically, because they happen when the PFD is driven out of its range, and small-signal approximations are no longer valid. However, simulation tools are useful to evaluate the transient behaviour of a PLL design from a cycle-slip perspective. The bandwidth is also linked to the phase margin of the PLL, which needs to be optimized for stability and speed. The stability, i.e. the phase margin, must be designed with some extra headroom for process variations, but also because it is often degraded in practical charge-pump PLLs by an extra capacitor that is added to the filter. The reason for this addition is to remove ripple on V_{ctrl}, created by imperfections in the PFD, that result in very short and often mismatched pulses on V_{ctrl}, even when the loop has stabilized. The maximum reasonable size of the extra capacitance is often set to be 20 % of C_1, which maximizes the phase margin of the PLL, if ζ is chosen to be around 0.7. Additionally, introducing an extra capacitance also sets a maximum value for R_1 in the loop filter [65] .

From the brief explanation above, it is clear that there are many degrees of freedom when designing a charge-pump PLL. As in any design, the target application has to decide the system requirements. The environment will set what output frequencies the PLL must be able to synthesize, what input reference sources are available, if fractional-N operation is necessary, if the VCO needs to have a direct I/Q output, if the PLL must provide an extra modulation possibility, or phase shifting capabilities, and much more. The considerations here also tie into considerations for the entire tranceiver. Additionally, even if the architecture is optimized, each individual subcircuit of the PLL must also be carefully designed.

Some notable published CMOS implementations of charge-pump PLLs for the mm-wave frequency range from recent years can be found in [55, 68–72].

In [68], a fractional-N PLL for 5G applications demonstrates state-of-the-art noise performance, and in [69], a quadrature 60-GHz PLL with an inductorless divider chain and an in-phase injection-coupled VCO is presented. A successful strategy used in PLLs for the 60-GHz band presented in [55,70–72] is to design the PLL for operation on a lower frequency. To reach the 60-GHz band [71] uses a frequency tripler after the VCO, [70] presents a sub-harmonic quadrature injection-locked VCO, and in [55] the third harmonic of the VCO in a 20-GHz PLL is extracted and boosted. The PLL in [72] operates at RF frequencies, at a few GHz, and uses a set of different multipliers to cover many mm-wave bands.

4.2.3 Charge Pumps

The charge-pump concept is presented in Fig. 22(a). The main concern in charge-pump design is how to minimize pulse mismatch, i.e. when the current waveforms of the UP and DN pulses are not perfectly matched. It leads to ripple, noise, and spurs in the PLL output frequency spectrum. The problem sometimes originates from unmatched signal delays from the PFD, but there are many possible inherent causes within the charge-pump that may exacerbate the mismatch. Fig. 24 shows a straightforward implementation of a charge-pump. Many variations exist, and propose different ways to deal with imperfections that cause mismatch.

In the charge-pump in Fig. 24, the PMOS switch needs to have an inverted signal on its input to switch on, and as a first precaution against time delay, the inverting buffer in the UP path is matched by a transmission gate in the DN path. Other inherent causes of mismatch are affected by the transistor geometries. The individual transistors of the charge-pump are often made very wide, so that they can deliver current even when V_{ctrl} is close to ground or VDD. Large devices will have more parasitic capacitance and more space for storing charge in their inversion layers. This charge will be absorbed by the current sources when they are on, and dissipated when they turn off, causing unwanted nonlinear effects. Another nonlinear effect in charge-pumps is channel-length modulation, which is more dominant in short-channel devices. The channel-length modulation leads to mismatch because as V_{ctrl} changes, so does the drain source voltage of the current sources. This effect will always make one current source more effective at pushing current, while the other is less effective. A popular technique for reducing current mismatch due to channel-length modulation is presented in [73] Finally, random mismatches and transistor noise in the charge-pump also play a part in the PLL.

4.2.4 Dividers

The division in the PLL is done in steps, and often one or more of the steps are programmable to enable the PLL to synthesize different frequencies without

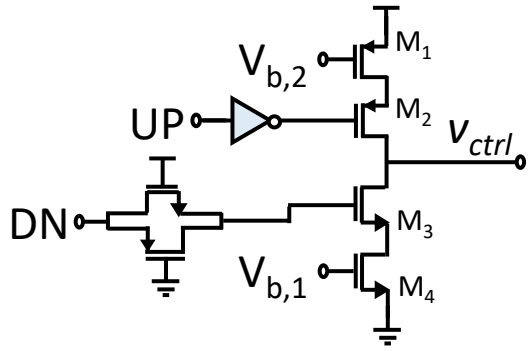


Figure 24: Charge pump transistor implementation.

having to change the input reference frequency. The most common choice for controlling these dividers is a sigma-delta modulator, which changes between division steps very fast and creates the desired frequency when averaged out. Closest to the PFD, the signal will have a lower frequency and more conventional digital divider designs can be used. At this position in the chain, the dividers can be programmable pulse-swallow dividers or dual-modulus dividers. Closer to the VCO, the frequencies that the dividers have to handle are higher. Faster logic is needed, such as current-mode logic (CML). A latch-based CML divide-by-two circuit is shown in Fig. 25 [74]. It is used in the divider chain of the PLL in paper V in this thesis, where it demonstrated good performance up to over 20 GHz.

When the divider speed needs to be even higher, as is the case of the first divider after a VCO that is operating at 60 GHz and above, a common choice is to instead turn to a tuned topology called injection-locked dividers (ILFDs). In their core they are similar to VCOs, and consequently often implemented as a cross-coupled VCO. To act as dividers, they are tuned to the divided output frequency, and the input signal to be divided is injected into the VCO in a way that makes it lock to it. Injection locking is of interest in many systems, and there are well-researched limits for when an injection lock can occur. The locking range for an ILFD is expressed as [75, 76]

$$\omega_{range} \leq \frac{\omega_0}{2Q} \cdot \frac{2}{\pi} \cdot \frac{I_{inj}}{I_{osc}} \tag{11}$$

where Q is the quality factor of the divider's LC tank, I_{inj} the magnitude of the injected current, and I_{osc} the magnitude of the free running oscillator current at f_0. It is clear that the more efficient the injection is, the wider the locking range becomes. A varactor can also be used in an ILFD to increase

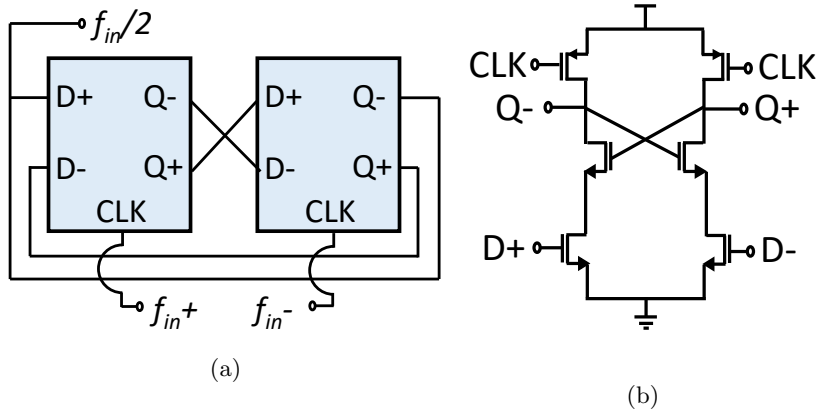
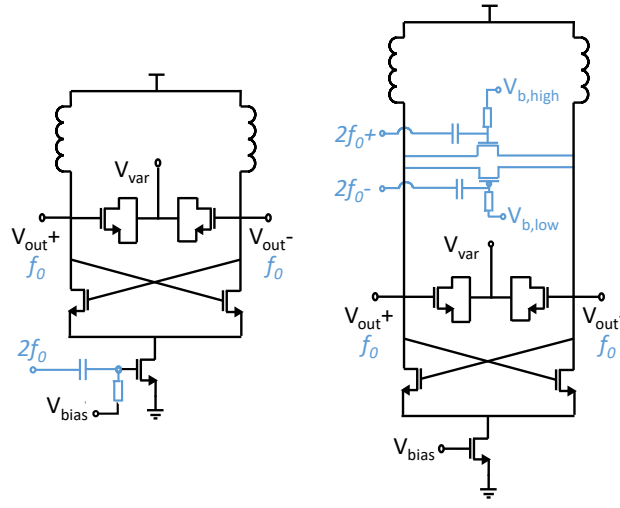


Figure 25: (a) High-speed latches in a tuned divide-by-two configuration. (b) Individual latch.

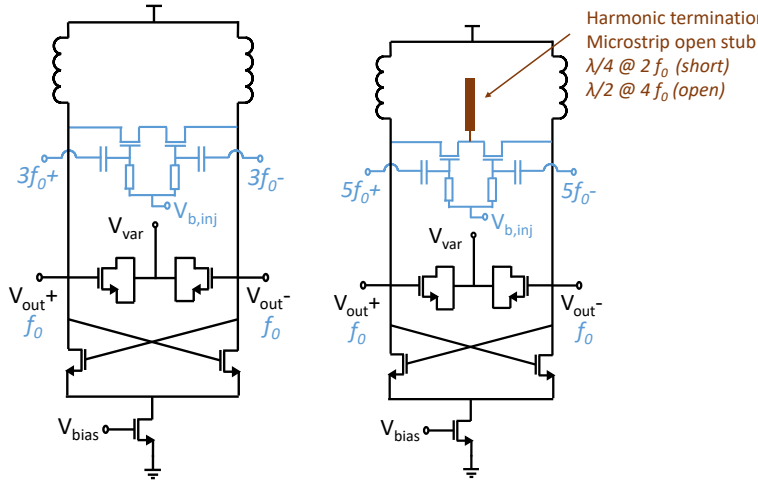
the locking range by tuning the circuit at the expense of complexity, loading of the tank, and larger chip area. Figure 26 shows two possible choices for injection of a signal at twice the output frequency. In the variation in Fig. 26(b), a differential signal is injected, which permits the use of the full output voltage swing of the preceding VCO. ILFD with higher division ratios have also been demonstrated. Figure 27(a) shows a divide-by-three ILFD. Here, the injected signal is at three times the self-oscillation frequency, and the transistors used for the injection will act as mixers and mix the input signal at $3f_0$ with the existing self-oscillation frequency f_0, creating even-order harmonics in the node between the injection transistors, where the second harmonic of the self-oscillation frequency naturally occurs [77]. A small change in this node, suppressing the second harmonic while favouring the fourth harmonic, as is shown in Fig. 27(b), makes the ILFD a divide-by-five circuit instead [78].

The output phase noise of an ILFD will generally be the same as the phase noise of the signal that it is locked on to, but it will increase at the edge of the locking range. Inside the locking range it will generally not introduce spurs, and because of its tuned nature, harmonics of the divided frequency will be suppressed.



(a) (b)

Figure 26: Injection-locked divide-by-two circuits. (a) Injection through the current source. (b) Direct differential injection.



(a) (b)

Figure 27: Injection-locked circuits. (a) Division-by-three. (b) Division-by-five.

Chapter 5

Paper Summary and Conclusions

This chapter presents summaries and conclusions of the results obtained in the included research papers. The author's contributions to each paper are also stated.

5.1 Summary

Paper I describes a two-stage, class-A PA for the 60 GHz ISM band. Each stage is differential and uses NMOS transistors in common-source configuration. To counteract the significant gate-drain capacitance at mm-wave frequencies, each stage is equipped with capacitive cross-coupling neutralization. It is implemented with NMOS transistors to ensure that it is matched to the transistors whose parasitic capacitances it should counteract. The input stage uses transistors that are dimensioned to cope with the large currents involved. The transistors of the subsequent output stage are 60 % larger. For measurement purposes, the PA has baluns at both the input and output, each carefully tuned to provide good input and output matching. Neither of the baluns are excluded from the calculations of the PAE. The inter-stage matching employs a 2:1 transformer, which is sufficiently wideband. The design was implemented in 65-nm CMOS and the manufactured chip was mounted on a PCB with bond-wire connections for bias and supply voltages. The mm-wave signals were measured using on-chip probing and a network analyzer. The chip photo is shown in Fig. 28. The input and output matching is at their best around 67 GHz, where the gain also peaks. The maximum gain is 16.8 dB and the 3 dB bandwidth is 9 GHz, enough to cover the ISM band at 60 GHz. Operating from a 1.2 V supply voltage, its peak PAE is 18.5 %, well above other two-stage PAs presented before it. It has a maximum output power of 11.8 dBm, and a 1-dB output-related compression point at 8.4 dBm.
Contribution: I did the analysis, simulations, layout, measurement setup, measurements, and the manuscript writing, under supervision of the second and third authors.

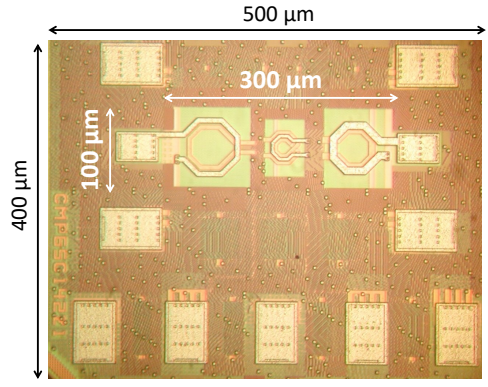


Figure 28: Chip microphotograph of the circuit in paper I.

Paper II describes a varactorless VCO, operating in the 60-GHz ISM band. At its core, it is a basic cross-coupled VCO. Instead of using a varactor for the frequency tuning, it changes the effective inductance seen by the cross-coupled NMOS transistors. This is achieved using an extra, in-phase branch, with its inductance placed right outside the coil of the primary inductance. The mutual inductance is dependent on the coupling factor and on the ratio between the currents in the two branches. The design was implemented in 65-nm CMOS and the manufactured chip was mounted on a PCB with bond-wire connections for bias and supply voltages. The mm-wave signals were measured with an on-chip probe, a spectrum analyzer, and a phase noise analyzer. The chip photo is shown in Fig. 29. Changing the currents in branch 1 and 2, and consuming 6-30 mA from a 1.2 V supply, the frequency can be tuned from 62.2 to 65.1 GHz. The measured phase noise stays flat across the tuning range, and hence the best FOM of -182.4 dB/Hz is found at the highest frequency, when the current consumption is at its lowest. In all, the circuit demonstrates that a varactorless structure can lead to good phase noise performance. However, the architecture inherently narrows the tuning range.

Contribution: I did the analysis, simulations, layout, measurement setup, measurements, and the manuscript writing, under supervision of the second and third authors.

Paper III presents an empirical study of the efficiency at 60 GHz of a well-known technique of suppressing phase noise in VCOs. Two cross-coupled VCOs are manufactured: one baseline VCO, and one identical design except for the added noise source filtering at the current source. The filtering is implemented

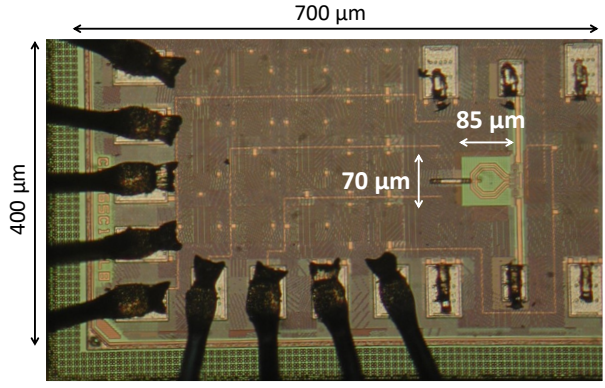


Figure 29: Chip microphotograph of the circuit in paper II.

with an inductance above the current source, tuned to twice the frequency of oscillation, to prevent the resistance of the cross-coupled pairs from loading the resonator in the switched stage. A capacitance is also inserted in parallel with the current source, providing a low-impedance path to ground for the noise generated in the current source. As this method of lowering the phase noise trades phase noise for area, it is especially interesting at 60 GHz, where inductors are small. However, the second harmonic will be at 120 GHz, closer to f_T and f_{max} of the technology, and it was not previously investigated if this would impact the efficiency of the method. Simulations show that the Q-value of the source inductance has a small impact on the efficiency, but the value of the inductance is more important. The VCOs were implemented in 28-nm FD-SOI CMOS and the manufactured chip was mounted on a PCB with bond-wire connections for bias and supply voltages. The mm-wave signals were measured with an on-chip probe, a spectrum analyzer, and a phase noise analyzer. The chip photo is shown in Fig. 30. At 0.9 V supply, both VCOs consume 3.15 mW, and the filtered VCO achieves a FOM of -187.3 dBc/Hz, which was state-of-the-art performance at the time of publication. Both VCOs have a tuning range of about 11 %, and even with the extra inductance in the filtering VCO, their areas are competitive. The improvement originating from the filtering was measured to between 5 and 12 dB across the tuning range.

Contribution: I did the analysis, simulations, and layout. The second and fifth authors did the measurements. I did the manuscript writing, with assistance from the second and third authors. All was done under the supervision of the last two authors.

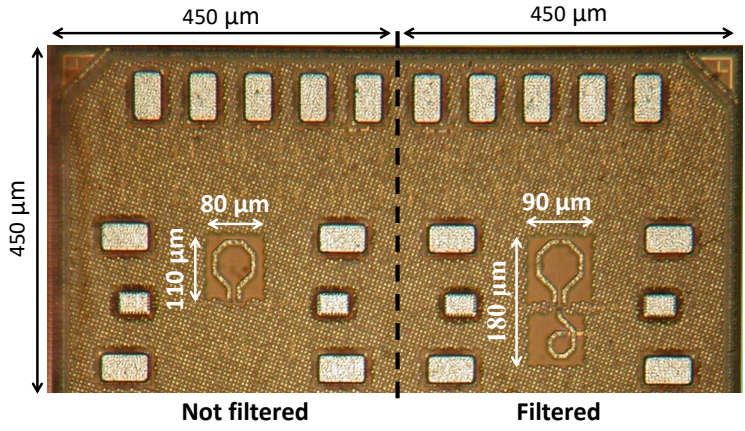


Figure 30: Chip microphotograph of the circuits in paper III.

Paper IV presents two ultra low-power VCOs for the 30 and 60 GHz bands. They both use a push-pull variation of the cross-coupled NMOS oscillator topology. The output voltage swing is restricted to the interval between 0 and VDD, which is lower than what can be achieved by the traditional cross-coupled architecture. Other potential drawbacks are that using a varactor for tuning may not be as efficient as in a basic cross-coupled topology, and that using two stacked transistors leaves less voltage headroom for the current source. The VCOs were implemented in 28-nm FD-SOI CMOS and the manufactured chip was mounted on a PCB with bond-wire connections for bias and supply voltages. The mm-wave signals were measured with an on-chip probe, a spectrum analyzer, and a phase noise analyzer. The chip photos are shown in Fig. 31. Both VCOs have tuning ranges around 11 % in their intended bands. The measured power consumption at 1 V for the 30 GHz VCO is 1.06 mW, and 1.35 mW for the 60 GHz VCO. Hence, they both demonstrate ultra-low power consumption, that is on par with, or even lower, than previously published sub-threshold VCOs, but without the need for an additional voltage domain. They both have excellent FOMs, -188.4 dBc/Hz for the 30 GHz VCO, and -186.2 dBc/Hz for the 60 GHz VCO.

Contribution: I did the analysis, simulations, layout, measurement setup, measurements, and the manuscript writing, under supervision of the second, third and fourth authors.

Paper V presents a mm-wave analog phase-locked loop with a VCO operating around 55 GHz, with very low power consumption and an improved lock time. The intended application for the PLL is integration into a 5G transceiver,

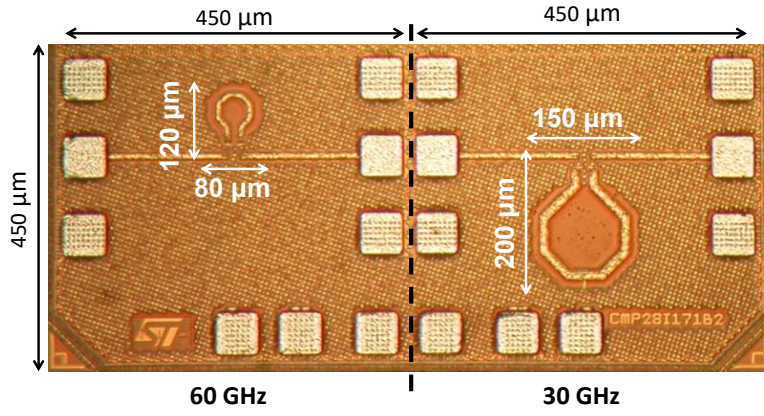
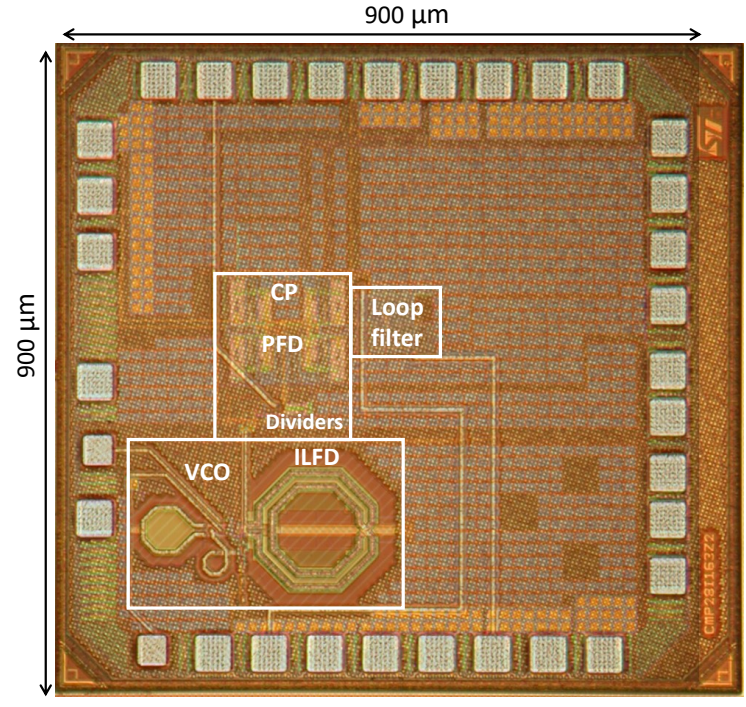
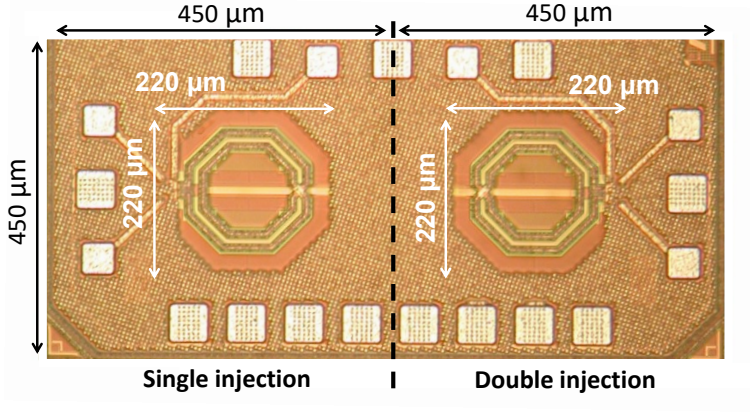


Figure 31: Chip microphotograph of the circuits in paper IV.

where another PLL for the RF bands already exists. This RF PLL can be used as the input for the mm-wave PLL and be responsible for channel selection and modulation, alleviating the demands of fractional-N division in the mm-wave PLL. At a first glance, the noise from the mm-wave PLL benefits from having a high input reference frequency of around 2.2 GHz, since the in-band noise adds as the division ratio squared. It also seems to imply that the PLL can use a higher bandwidth, and thus achieve a faster lock time. However, to keep the noise low, the bandwidth cannot be increased as much, and a low bandwidth coupled with a high reference frequency leads to cycle-slips and an excessively long lock-time. To address this problem, the proposed PLL employs a mode-shifting scheme, where it can operate in either a fast-locking or a low-noise mode. Both modes keep the same small-signal parameters, to ensure stability in both modes. When using the fast-locking mode to acquire a lock, the current in the charge pump is temporarily increased by a factor of 8, and the input reference frequency, as well as the divider chain in the PLL, are extended with divide-by-eight circuits. The PLL VCO uses the low-noise source-filtering design from Paper III. The VCO is followed by a divide-by-three injection-locked circuit. Traditionally, these are difficult to make wideband enough. However, the paper presents a novel double-injection topology that reuses the second harmonic present between the two injection transistors in parallel with the tank. This second harmonic signal is fed to the current source input, which creates a second injection path and increases the injection efficiency. Altogether, it makes the ILFD wideband enough to cover the whole VCO tuning range, while only consuming 0.5 mW. To verify the efficiency of the double-injection ILFD topology, two ILFDs are manufactured stand-alone, one with



(a)



(b)

Figure 32: Chip microphotographs of the circuits in paper V. (a) The PLL, overlayed with a semi-transparent layout. (b) The two versions of the ILFD.

and the other without the double-injection path, to facilitate a fair comparison. The PLL also includes a charge-pump with a novel current mismatch mitigation-technique based on negative feedback, and an improved operational amplifier that allows operation over a large common-mode range. Both versions of the ILFD, and the PLL, were implemented in 28-nm FD-SOI CMOS and the manufactured chips were mounted on PCBs with bond-wire connections for bias and supply voltages. The mm-wave signals were measured with on-chip probes, a spectrum analyzer, and a phase noise analyzer. The chip photos are shown in Fig. 32. Measurements of the two stand-alone ILFDs show that the locking range of the double-injection topology is almost doubled compared to the single-injection topology at a fixed varactor voltage and at the same power consumption. Measurements of the PLL show that it has a record low total power consumption of 10 mW. Together with an excellent integrated jitter of 176 fs, it achieves a FOM of -245 dB. Additionally, it has a lock time of 3 μs, demonstrating that the architecture can overcome problems with excessive lock time associated with a high input reference frequency.

Contribution: Together with the first author, I did the analysis, simulations, layout, measurement setup, measurements, and the manuscript writing. My primary responsibility was the mm-wave parts, but since no part of a PLL is independent of the others, we were both involved in all parts of the system. All was done under the supervision of the third and fourth authors.

Paper VI presents an injection-locked divide-by-two circuit for the 60 GHz band, stand-alone as well as integrated with the low-noise VCO from Paper III. The ILFD consists of a cross-coupled oscillator, which is injection locked by injecting a signal at around twice the frequency of self-oscillation. The efficency of the injection mechanism determines how wide the locking range is. To be able to use the full swing of a differential VCO, and create an efficent mechanism of injection, the signal is fed to the oscillator by direct differential injection. Simulations show that this creates a very wide locking range, which more than covers the tuning range of the VCO, even with process variations. One ILFD is integrated with the VCO to verify this. Both circuits were implemented in 28-nm FD-SOI CMOS and the manufactured chip was mounted on a PCB with bond-wire connections for bias and supply voltages. The mm-wave signals were measured with using on-chip probing, a spectrum analyzer, a phase noise analyzer, and a network analyzer. The chip photo is shown in Fig. 33. Measurements show that the widest locking range of 30 %, at -1.5 dBm of input power for the ILFD, is achieved at a power consumption of 4.3 mW from a 0.9 V supply. If the possibility to measure with even higher input power had been available, an even higher locking range could likely have been reported. Put together with the 60 GHz low-noise VCO from Paper III, the tuning range is set by the VCO to 10.2 %. The best measured phase noise from the VCO and ILFD combination is -111 dBc/Hz at 10 MHz offset from

the 28.5 GHz carrier.

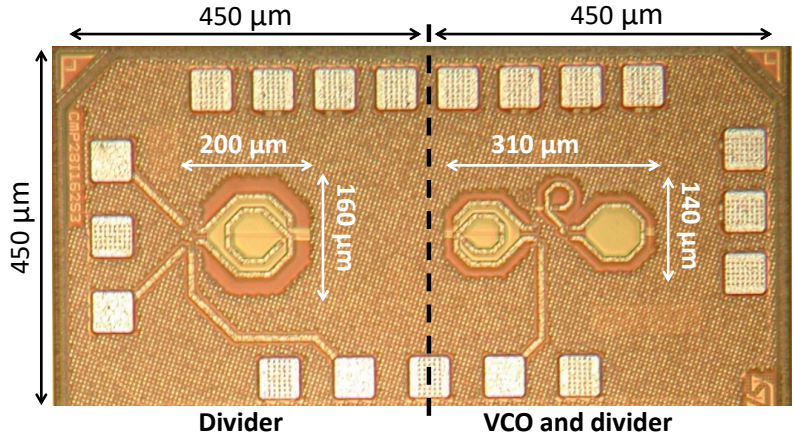


Figure 33: Chip microphotograph of the circuits in paper VI.

Contribution: I did the analysis, simulations, layout, measurement setup, measurements, and the manuscript writing, under supervision of the second, third and fourth authors.

Chapter 6

Discussion and Future Work

This dissertation presents several CMOS circuits that have been designed to be efficient parts of mm-wave transmitters. They have all been manufactured and verified by measurements.

A natural next step is to combine the different presented parts into complete, efficient transmitters. The presented PA, which demonstrates good performance when measured stand-alone, has already been integrated with mixers, a quadrature VCO and efficient injection-locked negative-resistance buffers into a sliding-LO transmitter for the 60 GHz band. It has been manufactured and my measurements show that the signal is properly upconverted and that the transmitter has wideband operation. However, the conversion gain is low. This was later confirmed in simulations to be mainly due to a mistuning of a passive structure, which reduces the input signal power to the PA. This structure could easily be re-tuned and manufactured again, as long as the silicon process is not discontinued. An improvement of this transmitter circuit should include a PLL with phase-shifting capability around the quadrature VCO, to make it viable for a 60 GHz beam-steering system.

The main drawback of the presented PLL is the limited tuning range. The most straightforward solution would be to increase it by increasing the size of the varactor, and thus accept the penalty of increased phase noise. However, the current-source filtering method used in the VCO to lower the phase noise could fit into many cross-coupled VCO topologies, also those a wider tuning range. At the same time, the PLL could also be extended to include phase-shifting possibilities by injecting current into the charge pump.

The PLL was designed to ultimately be a part of a whole homodyne transmitter for the 5G bands around 30 GHz. The signal from the 60 GHz VCO would be divided by the divide-by-two circuits presented in this thesis, to create a quadrature signal at 30 GHz. The dividers, which are low-power, have enough output power to directly drive a passive mixer for the upconversion. I have started this work and made initial simulations, but the transmitter still needs a power amplifier in the same technology node to be ready for manufacturing.

Finally, further integration with PCB antennas and on-chip high-speed DACs, in collaboration with other research groups, would be an interesting direction for future research.

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