CMOS Integration Based on All-III-V Materials

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I.INTRODUCTION

III-V based complementary metal-oxide-semiconductor (CMOS) circuits require additional development to achieve competitive p-type performance [1]. Antimonide-based materials such as GaSb demonstrate high hole mobility, and should be a viable alternative as channel material [2]. However, GaSb-transistor performance is currently limited by the gate-stacks [3]. Combinations of more traditional p-type SiGe channel combined with n-type III-V InGaAs channel has been suggested as an alternative to current CMOS technology [4]. To integrate this material system is not straightforward, mainly due to strong material selectivity during processing. InGaAs based circuits has gained traction for RF applications [5], thus all-III-V CMOS circuits are necessary for seamless integration with logic capabilities.

Here we co-integrate GaSb p-type and InAs n-type vertical nanowire MOSFETs with gate-all-around, using a common gate-stack. Specifically, the MOSFETs are based on vapor-liquid-solid (VLS) [6] grown InAs-GaSb heterojunction nanowires with a, highly doped, overgrown InAs shell for improved etch selectivity and contacts. The overgrowth enables fabrication with hydrogen silsequioxane (HSQ) spacers that are used for development of a self-aligned, gate-last, process compatible with vertical antimonide based structures. During processing, the shell is strategically removed to restore the proper channel material, namely the InAs or GaSb core material. All devices are heavily scaled with sub-100 nm gate lengths and gate diameters down to 20 nm, for the n-type device.

1 cm^2 p-type silicon (111) substrates with a 260 nm epitaxially grown, highly doped, InAs layer [7] are used for device fabrication. Subsequently, 15-nm-thick Au seed particles patterned by electron beam lithography (EBL) are utilized for growth of InAs-GaSb heterostructure nanowires. The nanowires are in-situ n- and p-doped by Sn and Zn respectively. 24 nm and 28 nm diameter Au dots are used for growing n-type wires and 44 nm for p-type wires [8].

II.RESULTS

Combined transfer and output characteristics for the n-type and p-type device are presented in Fig. 1. Transconductance $g_{m,peak}$ of 1.2 mS/µm for n-type and 74 µS/µm for p-type is reached while showcasing minimum subthreshold slope SS_{lin} of 74 and 271 mV/dec. The devices display enhancement mode operation with V_T = 0.08 and -0.02 V. Drain tunnelling, limiting the off-state, performance can be attributed to the narrow bandgap of InAs [9]. However, for the p-type GaSb device the large, gate-segment, diameter (40 nm) in combination with a non-optimal high-*k* interface degrades the off-state.

III.CONCLUSIONS

A co-integration process compatible with both InAs (n-type) and GaSb (p-type) MOSFETs has been developed. Highly scaled devices with sub-100 nm gate-lengths have been demonstrated using a common gate-stack, giving a $g_{m,peak}$ of 1.2 mS/um. P-type devices, demonstrating $g_{m,peak}$ of 74 uS/um, are also co-integrated on the same sample. Additional optimization of the GaSb gate-stacks combined with diameter scaling will improve the balance for the III-V CMOS.

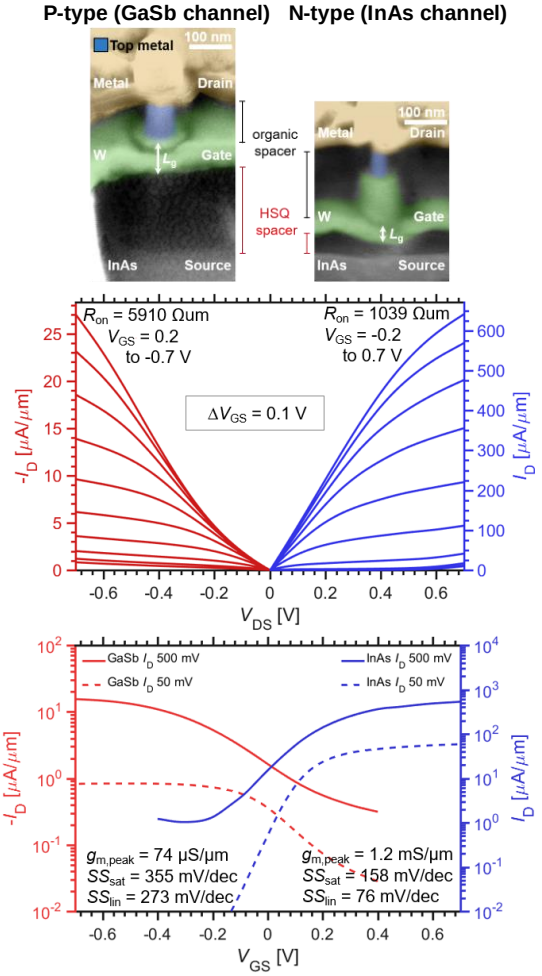

Fig. 1. Falsely colored FIB cross-section depicting single nanowires inside a p-type and n-type structure for, emphasizing the varied HSQ thickness. Transfer and output characteristics are presented for a selected p- and n-type device. The n-type device is comprised of 184 nanowire array with a pitch of 300 nm, diameter of 20 nm, and Lg = 50 nm . The p-type consists of 144 nanowires with a pitch of 350 nm, diameter of 40 nm, and Lg = 70 nm.

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