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An All-Digital ΣΔ-Frequency Discriminator of Arbitrary Order

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Abstract—In this paper, we propose an all-digital frequency synthesizer architecture, based on an all-digital ΣΔ-frequency discriminator. The new all-digital synthesizer is compared to previously published work. The architecture of the ΣΔ-frequency discriminator is verified using behavioral simulation.

Index terms— ΣΔFD, D/A, TDC, digitally controlled oscillator (DCO), frequency synthesizers, digital frequency synthesizer, fractional, all-Digital, sigma delta, phase domain, frequency discriminator, retiming, divider, quantizer.

I. INTRODUCTION

Rapid scaling of transistor feature size mandates the search for a new design style for analog and RF circuits. Exploiting the physical operation of the MOS device, i.e. a good switch, allows better utilization of MOS transistors in high frequency analog circuits. Such paradigm should facilitate the integration of analog and digital circuits on the same chip. Recently, an all-digital TX phase-domain phase locked loop frequency synthesizer was proposed [1][2]. The core of the synthesizer is a digitally controlled oscillator, DCO [3]. A simplified block diagram of this synthesizer is shown in Fig.1. Here, the concept of phase detection is based on accumulating the reference and DCO phase information and obtaining the phase difference through fixed-point subtraction [2]. In order to guarantee that phase detection is correct although the DCO and reference (REF) signals origin from different clock domains, reference retiming is adopted by sampling the reference edge using the DCO edge [2]. As a result of retiming, there is a fractional phase error that may degrade the overall resolution of the synthesizer. That is why a time-to-digital converter (TDC), was employed to correct this fractional error. In conjunction with the TDC circuit, an averaging real-time technique is used to calculate the DCO clock period and a circuit for calculating the inverse of a number [4]. These are used to normalize the fractional phase correction factor at the DCO output to one DCO clock period. This approach suffers from multiple disadvantages: the complexity and power consumption of the TDC in addition to the need of the inverse circuitry particularly that they operate at the DCO rate. Nonlinearities in the TDC circuit introduce spurs at the output of the synthesizer. High reference frequency (REF) is used to push the spurs far from the carrier. The need for high sampling frequency, in addition to the resolution being dependent on the number of stages, both make the TDC power hungry. In this work, we show that using ΣΔ-noise shaping techniques, we can avoid the use of a TDC and implement an all-digital noise-shaped frequency discriminator of arbitrary order. In the proposed architecture, improvement in fractional resolution is due to ΣΔ-noise shaping rather than fractional error correction using a TDC.
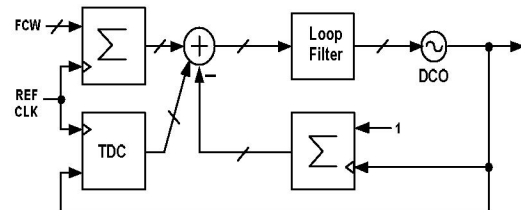

Figure 1. An All-Digital Phase-Domain Frequency Synthesizer

The paper is organized as follows: Section II introduces the new frequency synthesizer architecture. Section III details the architecture for our proposed ΣΔ frequency discriminator (ΣΔFD), and compares it to that published in [5]. In section IV, a divider-less version of our ΣΔFD is proposed. In section V, simulation results are demonstrated.

II. A ΣΔ DISCRIMINATOR-BASED ALL-DIGITAL PLL ARCHITECTURE

The proposed synthesizer architecture is shown in Fig.2. The core of the synthesizer is the ΣΔFD, which operates as a ΣΔ frequency-to-digital converter. It extracts the frequency of the DCO signal, compares it to a reference frequency (XREF), and produces a noise shaped digital bit stream whose average is proportional to the frequency error between the DCO and the XREF signals. The output bit stream is compared to the input frequency control word of the synthesizer (RFCW) in order to produce an error signal, on which the whole synthesizer operates, that is digitally filtered and then applied to the DCO to control the output frequency of the synthesizer. A similar architecture based on a second order ΣΔFD was previously published [6]. In [6], an analog

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voltage signal controls the oscillator. Therefore, a high resolution D/A is needed after the digital loop filter, which adds more complexity to the synthesizer. Extending that in [6] to a higher order noise shaper is possible at the price of adding analog components. A second order discriminator utilizing intensive analog blocks: charge pump, analog buffer and opamp comparator was reported in [5]. The main contribution of our work is an all-digital architecture implementing a $\Sigma\Delta FD$ that is extendable to higher orders with purely digital components. In this work, a DCO replaces the voltage controlled oscillator to implement an all-digital $\Sigma\Delta FD$-based synthesizer where the $\Sigma\Delta FD$ is of arbitrary order to enhance the frequency resolution.
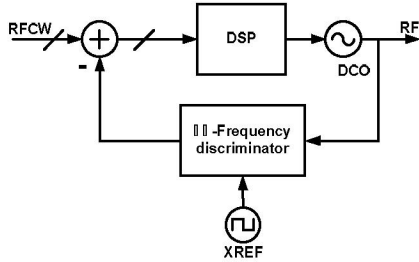

Figure 2. An All-Digital $\Sigma\Delta FD$-based Frequency Synthesizer

In the following section, we explain the operation of the $\Sigma\Delta FD$ in more detail. The proposed architecture is compared to previous work to show its advantages.

III. $\Sigma\Delta$-FREQUENCY DISCRIMINATOR

A. Principle of operation and previous work

The first published $\Sigma\Delta FD$ is shown in Fig. 3 [7]. The quantity that is $\Sigma\Delta$-modulated here is the period of the input signal. The input frequency is accumulated into phase. This phase signal is compared to a reference signal phase producing a phase error signal that is quantized to a single bit by the DFF. The shown loop acts as a first order noise shaper with a single bit quantizer. In [7], the phase error signal is not available, yet the DFF performs both the phase detection and quantization where its output is a binary digital voltage signal that indicates whether the signal phase leads or lags the reference phase.
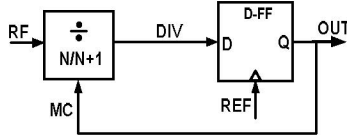

Figure 3. First order $\Sigma\Delta$ Frequency Discriminator [7]

Since the phase error signal is not available, direct extension of the architecture to higher orders to provide better noise shaping and higher frequency resolution is not straight forward. A single-loop 2nd order discriminator shown in Fig. 4 was implemented in [5], using a PFD for phase error detection and converting the phase error into an analog signal which is integrated using a charge pump, thus

providing second order noise shaping. This architecture suffers many drawbacks: First, its intensive use of analog blocks which are difficult to design and prone to process mismatches. Second, it uses a multi-modulus divider as result of the single loop implementation [5]. Third, is has nonlinearities due to PFD dead zone and charge pump leakage. Fourth, the charge pump, the comparator and the PFD all contribute to the overall output noise of the discriminator, especially the charge pump, which eventually degrades the resolution. Finally, extending this architecture to higher orders is not possible because it is difficult to control the stability of the loop using analog gains.

B. The new all-digital architecture

The block diagram of the proposed architecture is shown in Fig. 5 for a first order $\Sigma\Delta FD$. The divider acts as a phase accumulator. The phase detection circuit employs accumulation of the edges of the DIV and REF signals and simple arithmetic subtraction to produce the phase error. Thus, the phase error is available as a binary number. The quantization is achieved by simple truncation of the LSBs. Only the sign bit is used for modulus control. Retiming is employed to guarantee correct phase detection [2]. This is done by oversampling the external reference signal (XREF) by the input (RF) signal, to produce the retimed reference signal (REF) whose phase is the reference of the discriminator. It is worth mentioning that in [2] the result of the phase detection is the error signal that defines the resolution of the whole synthesizer and that is why the TDC was needed to correct for fractional errors due to retiming. But in our architecture, the phase error is already quantized, and the errors due to retiming are not significant, because the resolution is achieved through sigma-delta noise shaping and not phase detection accuracy as in [2].
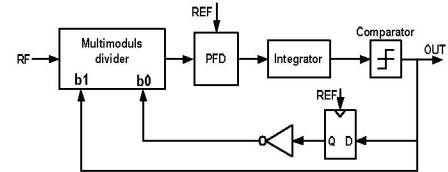

Figure 4. Single loop second order $\Sigma\Delta$ Frequency Discriminator [5]
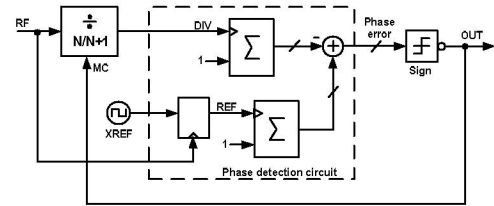
Figure 5. The new first order $\Sigma\Delta$ Frequency Discriminator

Another advantage of this circuit is that the phase error is available as a number. This allows extending the architecture to higher orders without need for analog blocks. A second order $\Sigma\Delta FD$ using this technique is shown in Fig. 6. The phase detection circuit is similar to that shown in Fig. 5. Only an extra digital accumulator is added to accumulate the

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phase error and provide second order noise shaping. It is straightforward to extend the $\Sigma\Delta$FD to higher orders using conventional $\Sigma\Delta$-modulators design techniques where scaling coefficients are designed to provide arbitrary signal transfer functions and noise transfer functions. In addition, a multi-bit discriminator can be easily implemented to provide higher resolution and larger dynamic range and improve stability by reducing quantizer overloading [8]. This is done by controlling a multi-modulus divider at the input with multiple bits of the phase error (for first order) or the accumulated phase error (for higher orders) instead of using the sign bit only. All the signals in the new $\Sigma\Delta$FD, except that for the divider, are represented as fixed-point numbers that cannot be corrupted by noise [9] whereas in [5], the charge pump is the main noise contributor in the discriminator. In [1] and [2], the TDC, is the only noise contributor in the phase detection technique.
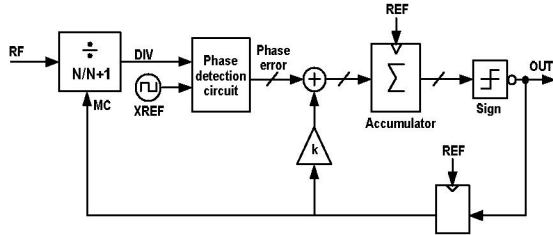

Figure 6. The new second order $\Sigma\Delta$ Frequency Discriminator

The proposed architecture can be easily modified into an all digital multistage noise shaper (MASH) $\Sigma\Delta$FD that avoids any delay mismatches compared to those reported in [10]. Since the phase error is available as a number, it can be fed to a second stage and then use an error combining circuit to produce the higher order noise-shaped bit-stream. A MASH 1-1 $\Sigma\Delta$FD is shown in Fig. 7. The second stage is simply a 1st order $\Sigma\Delta$-modulator. Similarly, we can produce any MASH architecture where the first stage is always a $\Sigma\Delta$FD and the next stages are $\Sigma\Delta$-modulators.
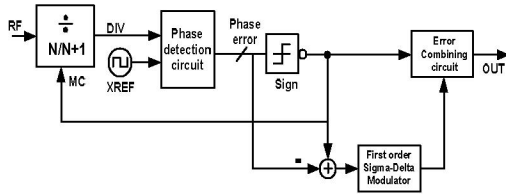

Figure 7. The new MASH 1-1 $\Sigma\Delta$ Frequency Discriminator

IV. DIVIDER-LESS $\Sigma\Delta$-FREQUENCY DISCRIMINATOR

By the same token of phase detection, the $\Sigma\Delta$FD can detect the phase difference between two signals at different frequencies using a small modification. The control word at the input of the accumulator clocked by the lower frequency is set to N, the ratio of the higher frequency to the lower frequency, instead of 1. This guarantees correct phase detection. This results in a divider-less architecture shown in Fig. 8. The frequency control word (FCW) is equal to N, which corresponds to the lower division factor of the divider

in Fig. 5. Now the feedback that governs the $\Sigma\Delta$–operation is achieved by simple addition. This architecture has two main advantages. First, multi-bit quantization does not add any complexity compared to the architecture in Fig. 5, which requires a multi-modulus. Second, the overall noise performance of the discriminator is improved because the divider is removed. Of course, this is at cost of the higher power consumption in the accumulator clocked by RF input.
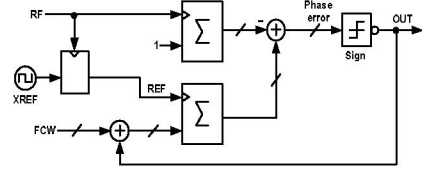

Figure 8. The Divider-less first order $\Sigma\Delta$ Frequency Discriminator

V. SIMULATION RESULTS

All simulations used behavioral Matlab models that capture finite word-length effects. In all simulations, the lower modulus of the divider is set to four, the reference frequency is 1.0 GHz, and the spectrum is calculated using $2^\wedge16$ FFT points with Blackman-Harris windowing. Fig. 9 shows the output PSD of the 1st and 2nd order $\Sigma\Delta$FDs shown in Fig. 5 and Fig.6 respectively. It is obvious that noise floor drops by about 5dB in the divider-less architecture case. This corresponds to 0.54 bits of resolution improvement. Fig.10 shows the output PSD of the MASH 1-1 2nd order $\Sigma\Delta$FD in Fig.7. Fig.11 shows a comparison for different values of the number of accumulator bits, N_{acc}. They are all compared to the case of ideal accumulator which is the top graph in Fig.11. In this figure all bit-streams are for input frequency equal to 4.036 Fref. It can be shown that $N_{acc} = 7$ is most similar to the ideal case. All graphs are similar in the steady state. But during the start-up, $N_{acc} = 7$ is the only curve that gives ideal response. The conclusion we have is that system dynamics are dependent on the number of accumulator bits, but $N_{acc} = 7$ is sufficient to give the required response. Fig.12 shows the response of the 2nd order $\Sigma\Delta$FD to an input frequency step equal to 0.8Fref. The $\Sigma\Delta$FD starts from a locked state at Fin = 4.1 GHz and jumps to $F_{in} = 4.9$GHz. Settling time is in the order of 60 ns, using $N_{acc} = 7$.
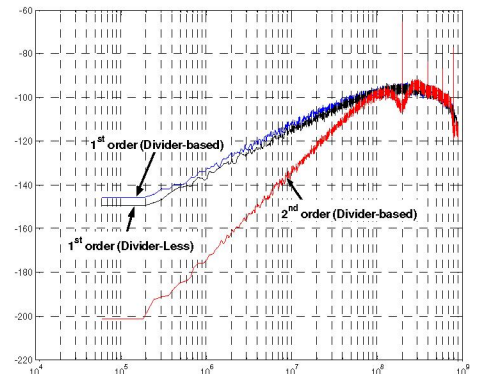

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Figure 9. Output PSD of the first and second order ΣΔ Frequency
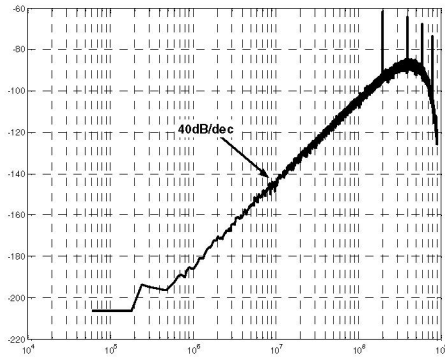Discriminators shown in Fig. 5, Fig. 6 and Fig. 8

Figure 10. Output PSD of the MASH 1-1 second order ΣΔ Frequency
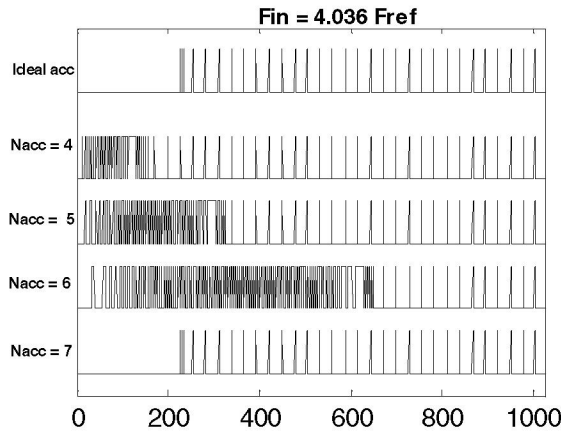Discriminator shown in Fig. 7

Figure 11. The output bitstream of the second order ΣΔ Frequency
Discriminator shown in Fig. 6 for different values of accumulator number
of bits (N_{acc})
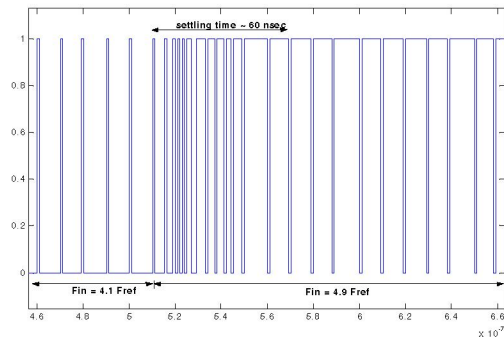

Figure 12. The output bit-stream of the second order ΣΔ Frequency
Discriminator shown in Fig. 6 showing response to an input frequency step
equal to 0.8Fref where N_{acc} = 7

VI.   CONCLUSIONS

A new, all-digital ΣΔFD architecture was introduced for use
in frequency synthesis. The proposed architecture has the
advantage of being extendable to higher orders, where the
design methodology is similar to that of conventional ΣΔ-
modulators. Thus, the STF and the NTF are arbitrary and can
be optimized to achieve a desired performance. In addition
the new architecture can be configured into MASH
structures. When has multiple advantages in the context of
frequency synthesizers. Compared to what was reported in
[2], the removal of the TDC simplifies the circuit and
reduces the sampling frequency because there are no spurs
due to TDC nonlinearities that need to be pushed to high
frequencies. This is in addition to the reduction in power
consumption, and the expected improvement in the overall
phase noise performance. In addition, a divider-less ΣΔFD
was proposed. It provides better noise performance and
makes multi-bit quantization easier because there is no need
for a multi-modulus divider.

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