LUND UNIVERSITY

Low-Temperature Front-Side BEOL Technology with Circuit Level Multiline Thru-Reflect-Line Kit for III-V MOSFETs on Silicon

Andric, Stefan; Ohlsson, Lars; Wenrersson, Lars Erik

Published in:
2019 92nd ARFTG Microwave Measurement Conference

DOI:
10.1109/ARFTG.2019.8637222

2019

Link to publication

Citation for published version (APA):
Andric, S., Ohlsson, L., & Wenrersson, L. E. (2019). Low-Temperature Front-Side BEOL Technology with Circuit Level Multiline Thru-Reflect-Line Kit for III-V MOSFETs on Silicon. In *2019 92nd ARFTG Microwave Measurement Conference: Next Generation Microwave and Millimeter-Wave Measurement Techniques and Systems, ARFTG 2019* Article 8637222 IEEE - Institute of Electrical and Electronics Engineers Inc.. https://doi.org/10.1109/ARFTG.2019.8637222

Total number of authors:
3

General rights
Unless other specific re-use rights are stated the following general rights apply:
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.
• Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
• You may not further distribute the material or use it for any profit-making activity or commercial gain
• You may freely distribute the URL identifying the publication in the public portal

Read more about Creative commons licenses: https://creativecommons.org/licenses/

Take down policy
If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

LUND UNIVERSITY

PO Box 117
221 00 Lund
+46 46-222 00 00

Low-Temperature Front-Side BEOL Technology with Circuit Level Multiline Thru-Reflect-Line Kit for III–V MOSFETs on Silicon

Stefan Andric, Lars Ohlsson, Lars-Erik Wernersson

Department of Electrical and Information Technology, Lund University, SE-221 00 Lund, Sweden (e-mail: stefan.andric@eit.lth.se)

***Abstract* — A multiline Thru-Reflect-Line (mTRL) calibration and parasitic pad removal kit is presented, intended for mm-wave III-V nanowire MOSFET characterization. Multiline TRL is implemented in a low-temperature BEOL process with substrate decoupled microstrip transmission lines. The transmission line characteristic impedance needed for accurate mTRL calibration is modelled. Simulated transmission line parameters show a good fit with measured transmission line data, including line characteristic impedance variation. Line loss less than 0.5 dB/mm up to 50 GHz is obtained. Finally, interconnect via section is calibrated and modelled, showing mTRL's ability to obtain small parasitic parameters.**

***Index Terms* — Back-End-Of-Line (BEOL), Benzocyclobutene (BCB), Microstrip Transmission Line, Nanowire MOSFET, On-wafer Calibration, Thru-Reflect-Line (TRL)**

I. Introduction

Characterization of intrinsic transistor performance at radio (RF) and millimeter-wave (mm-wave) frequencies poses a significant challenge [1]. Complications are related to instrument calibration and on-wafer deembedding techniques, where probing pad parasitics are removed from measured data. Device parasitics are easily misjudged due to non-ideal definition of reference standards in the complex environment of a monolithic circuit. In addition, most standards will deviate from ideal behavior with increasing frequency [2].

To address future transistor performance needs, III-V nanowire (NW) MOSFETs integrated on silicon (Si) are a promising candidate [3-4]. On the front-end-of-line (FEOL) level, their device contacts are typically defined on multiple levels in a dielectric environment. Even if thoroughly characterized at the FEOL level, RF circuit design takes place on the back-end-of-line (BEOL) level.

A device access structure, consisting of metallized vias, must be used to interface between FEOL devices and BEOL circuit environment. To provide maximum device performance at the circuit level, this access structure is required to provide low loss and minimal reactive parasitics. It must also support a well-defined calibration reference plane at BEOL level to yield data useful in circuit design. Furthermore, knowledge of the parasitic structure in the interface module connecting FEOL and BEOL allows for direct translation of performance between the two levels, accelerating the design cycle. Therefore, to maintain integrity and performance of scaled III–V NW MOSFETs, the BEOL must be fabricated at a limited thermal budget.

In this paper, we demonstrate the implementation of an RF BEOL compatible with the low thermal budget required by III–V NW MOSFET technology. Microstrip transmission line technology is utilized to implement a set of multiline thru-reflect-line (mTRL) calibration kits [5-7]. It offers high accuracy over a defined bandwidth, while maintaining simplicity in structural design. Initial modelling of the device interface module, connecting between FEOL and BEOL, is also evaluated.

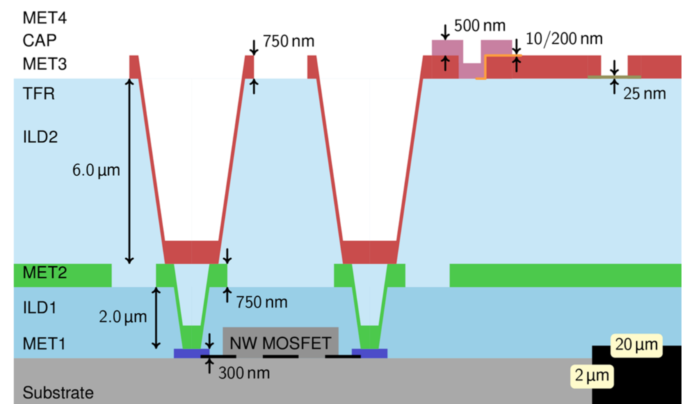

Fig. 1. Schematic BEOL dummy cross-section, showing metal (MET), interlayer (ILD), capacitor (CAP) and resistor (TFR) layers, including via structures to a NW MOSFET.

II. BEOL Fabrication and TRL Overview

A schematic cross-section of the implemented BEOL is shown in Fig. 1. It contains two interlayer dielectric (ILD) layers, four metal (MET) layers, one thin film resistive (TFR) layer, and one thin capacitive (CAP) layer. This front-side only RF BEOL is intended for co-integration on FEOL technologies utilizing III–V nanowire MOSFETs. The first interlayer dielectric provides separation between the device contacts (MET1) and the RF groundplane (MET2). A thicker interlayer dielectric (ILD2) supports microstrip transmission lines and passive devices formed in the top layers (TFR, MET3, CAP, and MET4), facilitating RF signal propagation, matching, and stabilization.

The interlayer dielectrics are realized by Dow Cyclotene™ spin coating and curing into benzocyclobutene (BCB), which has low relative dielectric permittivity, $\varepsilon_r = 2.7$. The layers

978-1-5386-6599-2/19/$31.00 ©2019 European Union

are cured in nitrogen ambient at only 250°C to preserve the III-V nanowire MOSFET technology. Interconnect vias are dry etched in O_2/SF_6 based RIE through a soft mask. All metal layers are deposited by thermal evaporation of Ti/Au through a lift-off mask. The thin film resistive layer is NiCr with a sheet resistance of 100 Ω/□, patterned by lithography and thermal evaporation in a lift-off process. Capacitors, deposited by means of low temperature ICP-PECVD and liftoff, are formed by sandwiching SiO_2 between the topmost metal layers. All lithography steps utilize soft UV exposures.

This simplistic fabrication scheme with a low temperature budget is compatible with our in-house III-V NW MOSFET technologies. It also allows co-integration on, e.g. high-density Si CMOS technologies enabling digitally-assisted mm-wave circuits with access to a low loss RF BEOL.

A. TRL Kit Description

The microstrip transmission line environment is ideal for front-side BEOL implementation. It decouples the RF signals from substrate effects (loss and mode coupling) by means of the groundplane. Transmission lines and discrete passive components are placed on the topmost BCB layer (ILD2). The groundplane is only opened at via positions to the substrate level and at 100 µm pitch RF probe pads. A tapered transition and a 100 µm line section is used to feed the calibration reference plane. This allows for evanescent mode decay and establishes well behaved quasi-TEM propagation.

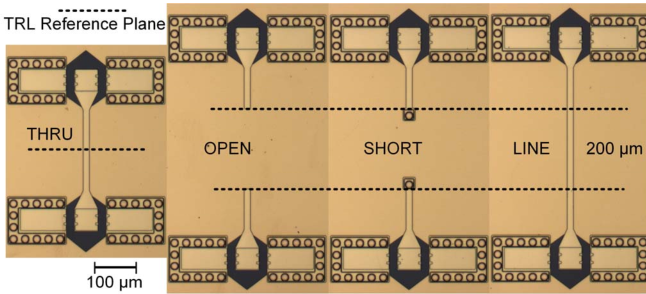

Fig. 2. Optical micrograph showing different TRL standards: THRU, OPEN, SHORT and 200µm long LINE standard, shown left to right, respectively, with marked calibration reference plane

A calibration kit with structures that support on-wafer mTRL has been fabricated, as shown in Fig. 2. The mTRL calibration procedure is based on a few basic structures. They consist of a "THRU" standard, where RF pads and access structures are connected back-to-back. By contrast, the individual reference planes of the "REFLECT" standards ("OPEN" and "SHORT") are separated by 200 µm to minimize crosstalk. Multiple "LINE" standards have also been fabricated. Their lengths yield the valid frequency band of the mTRL routine, loosely defined by the propagation phase range from 20° through 160°. Fabricated microstrip line lengths are 200 µm, 600 µm and 1mm, which, considering the approximate microstrip mode effective dielectric permittivity $\varepsilon_{eff} = 2.3$, corresponds to the bandwidth 10–440 GHz.

The mTRL calibration routine requires the characteristic impedance (Z_0) of the transmission line to be known per frequency. An incorrect impedance assumption leads to improper s-parameters scaling and deteriorated calibration accuracy. In general terms, the line impedance is

$$Z_0 = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}}, \tag{1}$$

where R', L', G', and C' are resistance, inductance, conductance, and capacitance per unit length, respectively, while $\omega = 2\pi f$ denotes angular frequency. These frequency dependent line parameters are found during calibration, under the assumption of a characteristic impedance, determined separately. We use values calculated by Keysight ADS for the specific geometry utilized, together with line DC resistivity measurement. Additionally, the line and dielectric parameters determine the propagation constant

$$\gamma = \sqrt{(R' + j\omega L')(G' + j\omega C')} = \alpha + j\beta, \tag{2}$$

where α is the attenuation and β is the phase constant. It is derived from TRL measurements directly and only assumes invariant error boxes connecting to the reference plane.

B. Measurement Procedure

The fabricated structures are measured up to 67 GHz using Cascade i67 100µm-pitch GSG probes, and a Rohde&Schwarz ZVA67 vector network analyzer. The first-tier LRRM instrument calibration is done using a Cascade impedance standard substrate (ISS 109-101C). A second-tier mTRL calibration is then performed, which sets the reference plane shown in Fig. 2. The probing setup is then ready for the circuit level device measurements. Device research typically includes further deembedding measurements, providing access to intrinsic FEOL device data, excluding the interface structure parasitics. All measurement data is processed in Cascade WinCal 4.6.

The first-tier calibration is performed initially in order to evaluate performance of on-wafer standards, prior to second-tier calibration. After the first-tier instrument calibration with the off-wafer calibration kit, the on-wafer mTRL kit is measured in a specific order: THRU, OPEN, SHORT, LINE1, LINE2, and LINE3, as a part of a second-tier calibration. For successive standards, the distance between probes has to be changed. This is a drawback of the TRL calibration, where any change of the distance between probes changes cross-talk terms in the error box. Increased redundancy compensates for possible crosstalk errors due to spacing variation between probes, providing robustness. To enable this, the dual REFLECT standards (OPEN and SHORT), and several LINE standards with different lengths are utilized in mTRL.

III. Results And Discussion

A. Transmission Line Parameters

A microstrip transmission line cross-section with all relevant dimensions is shown in Fig. 3(a). The line width is set to 16 µm, which corresponds to the characteristic impedance of approximately 50Ω. This is a line design in one of the mTRL calibration kits. The mTRL kits were fabricated on both semi-insulating InP and high-resistivity Si substrates to verify the effectiveness of the microstrip groundplane. As shown in the measured data in Fig. 3(b), no significant contribution from substrate is present in attenuation. Fig 3(b) also shows that the transmission line model generated by ADS gives a good fit to the measured data, using a dielectric loss tangent, $\tan\delta_{BCB} = 10^{-2}$ for the BCB. The resulting attenuation constant of 0.5 dB/mm at 50 GHz is comparable to other BCB-based processes in use today [8-9].

The attenuation at low frequency is governed by metal loss, as expected. However, the measured attenuation exhibits a slope transition, approximately above 30 GHz. This can be attributed to Debye-type dielectric relaxation centered at frequencies far above the measurement range, dominating over the total loss at high frequencies. One possible explanation is the low BCB curing temperature which can result in the polymerization rate less than 100% [10]. Additionally, groundplane opening beneath probe pads could cause complex behavior in attenuation. However, as seen from Fig. 3b, there is no significant substrate effect present. Therefore, further investigation is needed to determine the loss mechanism. Finally, we attribute the periodic ripple to cable movements during TRL measurements, while deviations around 55 GHz correspond to probe placement variability on the measurement pads.

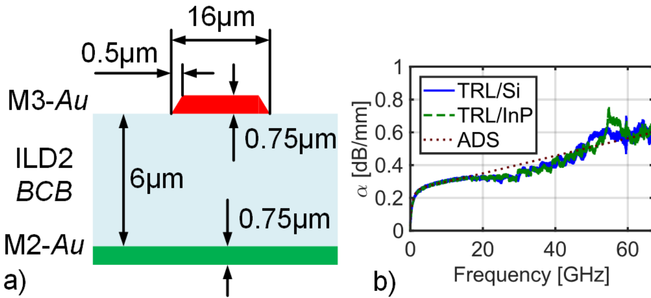

Fig. 3. a) A 50Ω microstrip line cross-section (not to scale) showing line (red) and groundplane (green), separated by the thick interlayer dielectric (blue) layer and b) measured and simulated attenuation constant for microstrip lines on Si and InP substrates.

A range of line impedances are necessary in RF and mm-wave circuit design. To evaluate the implemented design environment further, TRL kits with line width variation were fabricated. Fig. 4(a-b) shows measured and modelled components of the propagation constant for line widths of 8µm, 16µm, and 43µm, which correspond to approximately 75Ω, 50Ω, and 25Ω, respectively. The agreement between measured and simulated data shows that the ADS model can be applied to a wide range of line dimensions, and that measured line parameters are acceptably captured by the model used. Distributed line parameters are also found in reasonable agreement, as shown in Fig 4(c-f), which follows from assuming the characteristic impedance from ADS for the TRL data. We attribute the deviations in distributed resistance and especially the complex behavior of the conductance at low frequency to limited models of skin effect and dielectric loss.

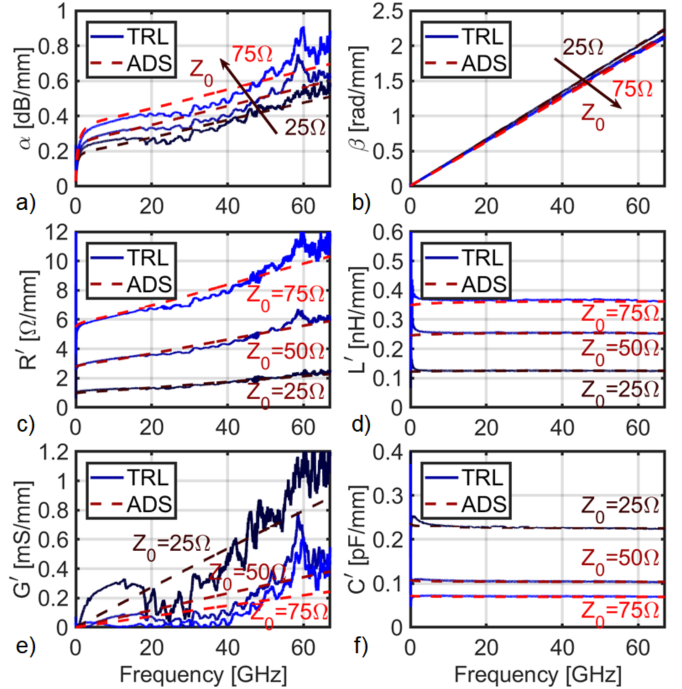

Fig. 4. a) Measured and simulated line attenuation constant, and b) phase constant vs frequency, with respect to the characteristic impedance Z_0 = 25Ω, 50Ω, and 75Ω; c) Measured and simulated line distributed resistance, d) inductance, e) conductance, and f) capacitance per unit length; with respect to the characteristic impedance Z_0 = 25Ω, 50Ω, and 75Ω

B. Component Calibration and Deembedding

The second-tier mTRL calibration establishes a microstrip reference plane on-wafer. Effectively, the RF probing pads, signal line tapering, and access microstrip line are calibrated out. This enables precise circuit level parameter derivation in the frequency band of interest for BEOL design. However, device studies also require deembedding of the stacked-via interface structure between BEOL and FEOL.

A scanning electron microscope (SEM) image of a measured stacked via structure on Si substrate is shown in Fig. 5(a). It illustrates how the metal layers contact from MET3 by MET2 down to MET1 layer. The structure has been fabricated and measured with RF probing pads and access lines, which are then effectively removed with the mTRL calibration. A calibrated measurement to simulation

comparison of a “MET1-OPEN” deembed structure is shown in Fig. 5(b). It describes the response of two stacked vias with an underlying, non-connected MET1 pad, which would be used as part of a standard two-step deembedding technique [11].

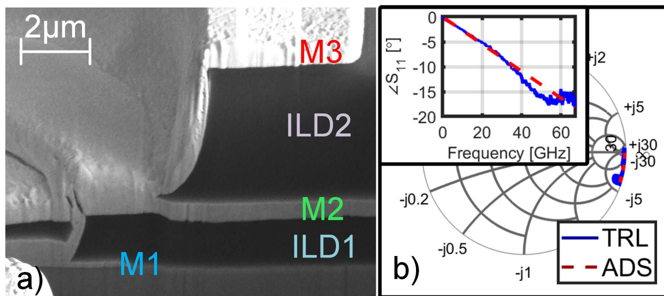

Fig. 5. a) SEM image of via structure connecting MET3, MET2 and MET1 layer; b) Simulated and measured reflection coefficient (s_{11}) and phase (inset) vs frequency, of stacked via structure terminated with “MET1-OPEN” standard

Modelling the structure, via resistance is estimated with DC measurements. For a total capacitance estimation, individual via capacitance is separately calculated, as well as capacitance between all neighboring segments, which are not belonging to individual vias. Self-inductance of individual metal segments have also been considered [12]. This quasi-physical model, consisting of lumped components implemented in ADS, shows good agreement to the measurements. The effective capacitance seen from the reference plane is $C_{via} = 8fF$, a relatively low value. We, once again, attribute parts of the deviations about 55 GHz to probe placement, but also to the complex mode matching problem; a transition from BEOL quasi-TEM microstrip mode to FEOL point contacts. This second-order effect needs to be evaluated further.

IV. Conclusion

An mTRL calibration kit has been presented using a simple BEOL design with low-temperature processing scheme. As part of the mTRL calibration kit, microstrip transmission line parameters were measured and a model has been implemented to simulate the line performance. Microstrip lines show less than 0.5 dB/mm loss at measured frequencies up to 50 GHz, while simulations are able to predict line behavior when line width is varied. The implemented RF BEOL was also verified to not depend in the underlying substrate. This promises successful integration on a variety of FEOL technology platforms. As proof-of-concept, small interconnect vias were measured and corrected with mTRL, showing good fit to a physical model used to describe via behavior. This low loss RF and mm-wave environment is henceforth universally available for future circuit design, as well as complex device and circuit characterization, such as III-V nanowire MOSFETs on Si.

Acknowledgement

This work has been supported by INSIGHT, European Commission’s Horizon 2020 Research and Innovation Action, under Grant Agreement 688784, and SSF, Swedish Foundation for Strategic Research.

References

[1] D.F. Williams, A.C. Young, and M. Urteaga, “A Prescription for Sub-Millimeter-Wave Transistor Characterization,” in *IEEE Transactions on Terahertz Science and Technology,* vol. 3, no. 4, pp. 433 - 439, July 2013.

[2] D.F. Williams, P. Corson, J. Sharma, H. Krishnaswamy, W. Tai, Z. George, D. Ricketts, P. Watson. E, Dacquay, and S.P. Voinigescu, “Calibrations from Millimeter-Wave Silicon Transistor Characterization,” in *IEEE Transactions on Microwave Theory and Techniques,* vol. 62, no. 3, pp. 658 - 668, Mar 2014.

[3] S. Johansson, E. Memisevic, L.-E. Wernersson, and E. Lind, “High-Frequency Gate-All-Around Vertical InAs Nanowire MOSFETs on Si Substrates,” in *IEEE Electron Device Letters,* vol. 35, no. 5, pp. 518 - 520, May 2014.

[4] C.B. Zota, F. Lindelöw, L.-E. Wernersson, and E. Lind, “High-frequency InGaAs tri-gate MOSFETs with f_{max} of 400 GHz,” in *Electronics Letters,* vol. 52, no. 22, pp. 1869 - 1871, Oct. 2016.

[5] G.F. Engen and C.A. Hoer, “Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer,” in *IEEE Transactions on Microwave Theory and Techniques,* vol. 27, no. 12, pp. 987 - 993, Dec. 1979.

[6] R.B. Marks, “A multiline method of network analyzer calibration,” in *60th ARFTG Conference Digest, Fall 2002.*, Washington, DC, USA, Dec. 2002.

[7] D.C. DeGroot, J.A. Jargon and R.B. Marks, “Multiline TRL Revealed,” in *IEEE Transactions on Microwave Theory and Techniques,* vol. 39, no. 7, pp. 1205 - 1215, July 1991.

[8] M. Urteaga, Z. Griffith. M. Seo, J. Hacker, and Mark J.W. Rodwell, ” InP HBT Technologies for THz Integrated Circuits," in *Proceedings of the IEEE*, vol. 105, no. 6, pp. 1051 - 1067, June 2017.

[9] T. Merkle, A. Leuther, S. Koch, I. Kallfass, A. Tessmann, S. Wagner, H. Massler, M. Schlechtweg, and O. Ambacher, ” Backside Process Free Broadband Amplifier MMICs at D-Band and H-Band in 20 nm mHEMT Technology," in *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, La Jolla, CA, USA, Oct. 2014.

[10] S. Sivoththaman, R. Jeyakumar, L. Ren, and A. Nathan, ” Characterization of low permittivity (low-k) polymeric dielectric films for low temperature device integration," in *Journal of Vacuum Science & Technology A*, vol. 20, no. 3, pp. 1149–1153, May/June 2002.

[11] M.C.A.M. Koolen, J.A.M. Geelen, M.P.J.G. Versleijen, “An improved de-embedding technique for on-wafer high-frequency characterization,” in *Proceedings of the 1991 Bipolar Circuits and Technology Meeting*, Minneapolis, MN, USA, Sept. 1991..

[12] E.B. Rosa, ”The Self and Mutual Inductances of Linear Conductors," in *Bulletin of the Bureau of Standards*, vol. 4, no. 2, pp. 301–344, 1908.