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Vertical InAs/InGaAs Heterostructure MOSFETs on Si

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ABSTRACT. III-V compound semiconductors offers a path to continue Moore's law due to the excellent electron transport properties. One major challenge, integrating III-Vs on Si, can be addressed by using vapor-liquid-solid grown vertical nanowires. InAs is an attractive material due to its superior mobility, although InAs MOSFETs typically suffer from band-to-band tunneling caused by its narrow band-gap, which increases the off-current and therefore the power consumption. In this work, we present vertical heterostructure InAs/InGaAs nanowire MOSFETs with low off-currents provided by the wider band-gap material on the drain side suppressing band-to-band tunneling. We demonstrate vertical III-V MOSFETs achieving off-current below 1 nA/μm

while still maintaining on-performance comparable to InAs MOSFETs, therefore this approach opens a path to address not only high-performance applications but also Internet-of-Thigs applications that require low off-state current levels.

Vertical vapor-liquid-solid (VLS) grown nanowires offer an interesting option for future electrical and optical devices, as the vertical growth direction allows a high degree of freedom in material selection. Thin nanowires can relax stress originating from lattice mismatch by lateral expansion, therefore high quality axial heterostructures as well as nanowires integrated on different substrates can be grown [1-4]. One major driving force for the development has been the possibility to integrate high mobility and direct band gap III-V materials on Si [1, 4, 5]. Axial heterostructures further offer the possibility for band gap engineering, which allows for design of advanced metal-oxide-semiconductor field-effect transistors (MOSFETs) [6, 7] and tunnel field-effect transistors (TFETs) [8-10], where for instance the tunneling current can be controlled by proper band gap engineering.

III-V MOSFETs integrated on Si substrates, such as InAs and InGaAs, are considered to extend Moore's law, as they offer the possibility to decrease the supply voltage and therefore power consumption, while still operating with a high performance [11, 12]. Continuous scaling of the gate length has led to an increase in the off-state power consumption due to leakage and, unfortunately, the problem is even worse for narrow bandgap III-V MOSFETs, which have relatively large off-currents due to band-to-band tunneling and impact ionization. The established way of comparing different digital technologies is to define the on-current (I_{on}) at a fixed off-current (I_{off}). III-V MOSFETs normally reach only the high performance limit (I_{off} = 100 nA/μm) due to leakage associated with the narrow band gap. Recently, planar MOSFETs with a wider

band-gap material on the drain side have demonstrated to decrease the output conductance, increase the breakdown voltage, and suppress the tunneling off-state leakage current to reach the standard performance limit (I_{off} = 1 nA/μm) [6, 7].

In this paper, growth, material characterization, processing, and device measurements of vertical InAs / $In_{0.7}Ga_{0.3}As$ nanowire MOSFET integrated on Si are presented. The wider band gap material, inserted as a segment on the drain side, together with the drain contact being electrically isolated from the substrate allows a decrease in the off-state leakage, while still maintaining the excellent transistor properties provided by the InAs channel. With the removal of the substrate leakage component, all of the drain current passes through the nanowire and it is therefore well controlled due to the excellent electrostatics provided by the gate-all-around (GAA) structure. We present MOSFETs with typical I_{off} between 1 and 10 nA/μm, with the smallest I_{off} below 1 nA/μm. This represents the first demonstration of vertical III-V nanowire MOSFETs achieving I_{off} = 1 nA/μm at V_{DS}=0.5V. These MOSFETs also have, to the best of the authors' knowledge, the highest high performance I_{on} (330 μA/μm at I_{off} = 100 nA/μm and V_{DS} = 0.5) demonstrated for vertical nanowire MOSFETs. The high I_{on} is related to a high g_m = 1.4 mS/μm as well as a good subthreshold swing SS = 85 mV/dec.

The MOSFETs were fabricated on p-type silicon substrate that had 300-nm-thick metalorganic vapor phase epitaxy (MOVPE) grown n-doped InAs layer, which acts as a seed layer for nanowire definition and a source contact for the transistors. The growth of the InAs thin film on Si have been demonstrated before with good electrical performance [13]. The nanowires were grown by MOVPE using electron beam lithography defined (EBL) gold particles in VLS growth mode (detailed description in methods). Three different diameters of EBL defined gold particles, 32 nm, 36 nm, and 40 nm, were used. The nanowires consisted of, starting from the substrate, a

segment with 100 nm unintentionally doped InAs, a 50-nm-long unintentionally doped graded InGaAs segment (from InAs to $In_{0.7}Ga_{0.3}As$), and 300 nm highly n-doped $In_{0.7}Ga_{0.3}As$, which also overgrew the undoped region forming a core-shell heterostructure. The analysis of the structure is shown in figure 1. The diameter of the core is a few nanometers larger than the gold particle diameter and the shell thickness is approximately 10 nm.

A scanning electron micrograph image, a transmission electron micrograph image, and a composition analysis of the nanowire are shown in figure 1. Typically, nanowires grown under these conditions have a wurtzite crystal structure, however the transition from InAs to InGaAs causes the formation of a short, approximately 10 nm long, zincblende segment at the InAs/InGaAs junction, which could be due to a variation in gold particle size induced by the Ga introduction [14]. Another clearly visible property, is the large number of stacking faults in the doped InGaAs segment, which could lead to a mobility degradation.

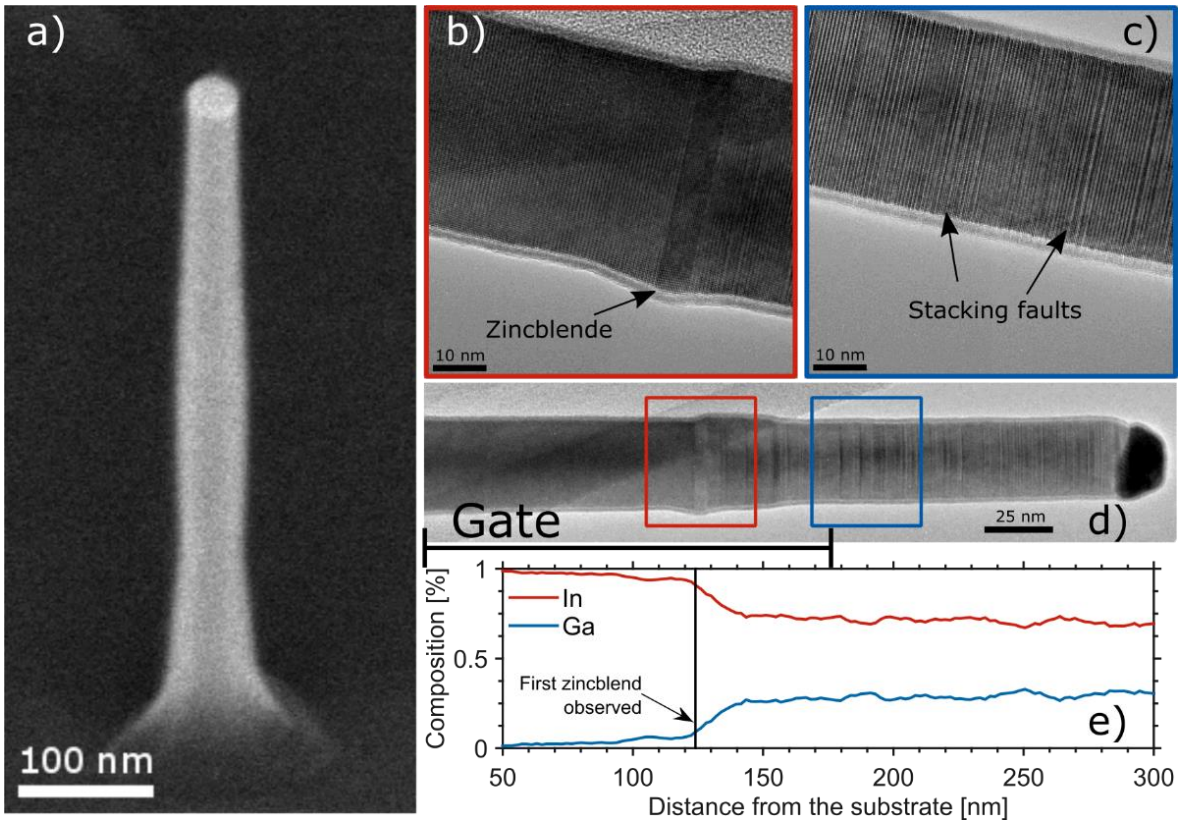

Figure 1. SEM (a) and TEM (d) images of the InAs/InGaAs heterostructure nanowire. TEM image (b) reveals short a zincblende segment at the heterojunction and a large amount of stacking faults (c) after doping is introduced. Composition analysis (e) shows that nanowire has an approximately 50-nm-long segment, where InAs is graded to $In_{0.7}Ga_{0.3}As$.

A schematic illustration of the transistor structure together with the false-color SEM image of a vertical nanowire are shown in figure 2. The transistor has a 50-nm-thick SiO_2 first spacer, a 5-nm-thick Al_2O_3/HfO_2 bilayer gate oxide, and a 60-nm-thick W gate. The transistor processing followed the recently developed gate-last process [15], where the gate is self-aligned to the source and drain regions, by a W top-metal and a doped shell at the bottom, as shown in figure 2 (detailed process description in methods). This alignment allows removal of the ungated regions, in which the transport would greatly increase the parasitic source and drain resistance and therefore decrease the transistor performance. Furthermore, to improve the transistor

electrostatics, the doped shell is removed from the channel region and the channel diameter is decreased to form a recess gate.

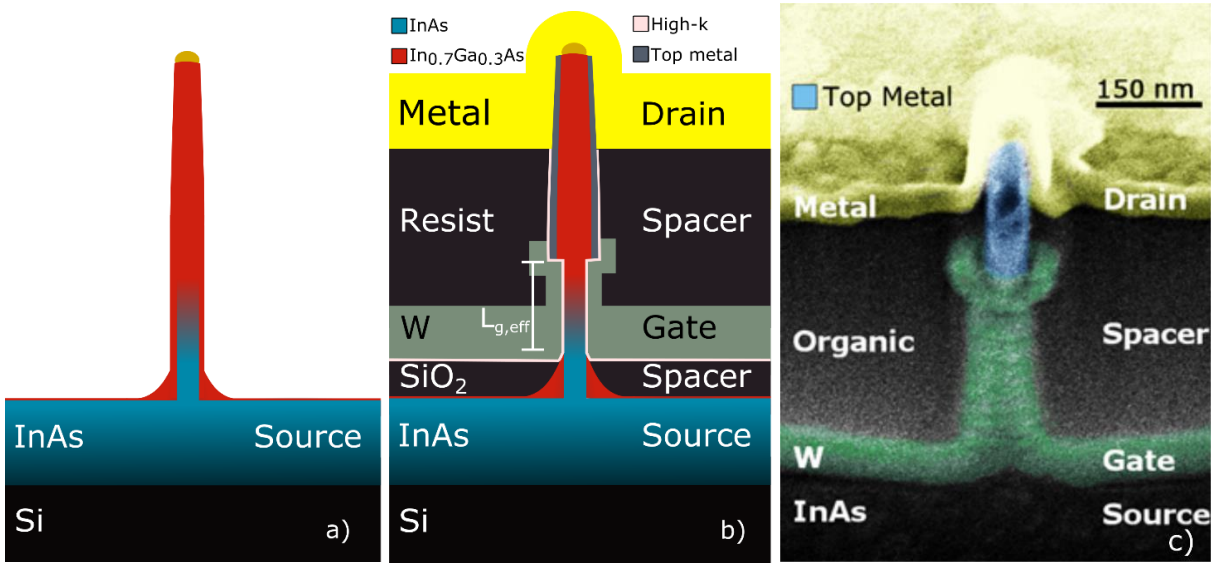

Figure 2. Schematic illustration of the nanowire after growth (a), finalized device (b) and a cross-sectional SEM image (c) of vertical InAs/InGaAs MOSFETs. The self-aligned gate technology together with the recessed gate allows to achieve high performance transistors.

Transfer characteristics of the vertical InAs/InGaAs single nanowire MOSFET at V_{DS} = 0.5 V is shown in figure 3a. The diameter of the nanowire, for this particular device, is 28 nm and the total gate length is 260 nm, where the effective gate length ($L_{g,eff}$), defined by the region where the nanowire thickness is uniform and the smallest (figure 2b), is 160 nm. In this work, only single nanowire transistors are demonstrated, as larger arrays always have slightly degraded performance due to small variations within the array. The transistor operates as an enhancement mode transistor with a threshold voltage (V_T) of 0.16 V (defined by extrapolating from the maximum g_m), a maximum transconductance (g_m) of 1.4 mS/µm (normalized by the circumference of the nanowire) and subthreshold swing (*SS*) of 85 mV/dec. The transistor shows good combined on- (g_m) and off- (*SS*) performance with a Q-value (g_m /*SS*) of 16, which is

required to achieve a high I_{on}. The best I_{on} of these transistors at I_{off} = 100 nA/µm and V_{DS}=0.5 V is 330 µA/µm. These transistors also show excellent I_{off} control due to the wider band gap on the drain side and GAA structure, therefore demonstrating vertical III-V nanowire MOSFETs achieving standard performance limit (I_{off}=1 nA/µm) at V_{DS}=0.5 V. For the best device, the I_{on} = 88 µA/µm at I_{off} = 1 nA/µm and V_{DS}=0.5 V was measured.

In figure 3b, the transfer characteristics of InGaAs and InAs drain MOSFETs are compared. The InAs/InGaAs MOSFET corresponds to the transistor in figure 3a whereas the InAs MOSFET is a similarly processed single nanowire vertical MOSFET with a diameter of 31 nm and a gate length of 170 nm. The maximum g_m of the InAs transistor is 0.75 mS/µm and *SS* is 95 mV/dec. Its Q-value is approximately 8 and therefore the performance corresponds well to recently published state-of-the-art vertical InAs transistors[15]. The InAs MOSFET has I_{on} = 183 µA/µm at I_{off} = 100 nA/µm and V_{DS}=0.5 V, which to the authors knowledge is the highest reported I_{on} for vertical InAs MOSFETs. From the data presented in figure 3b, it is clear that the transconductance g_m in the InAs/InGaAs MOSFET is considerably higher and the *SS* lower as compared to the InAs MOSFET. The ambipolar leakage component observed at negative gate biases is lower for the InAs/InGaAs MOSFET as compared with the InAs transistor and therefore lower off-state currents can be achieved when the InGaAs drain is introduced. The higher g_m and higher maximum on-current for InAs/InGaAs MOSFETs is based on a good balance between on- and off-state performance. For the comparison, vertical InAs device with the highest Q-value was selected. Vertical InAs devices with higher g_m and higher maximum on-current have been previously demonstrated, however they do not have reasonable off-state performance [16].

Figure 3c shows output characteristics of the MOSFETs with InGaAs drain. The MOSFET with InGaAs drain shows good saturation at relatively high V_{DS} values (< 1.2 V). Typical InAs

MOSFETs are not measured at high V_{DS} [5, 17-21], as impact ionization and band-to-band tunneling cause breakdown well below 1 V. Therefore, this technology is attractive for RF applications as the current is saturated over a relatively large region. The difference in the increase of the leakage current with drain bias, which will evidently also cause the device breakdown, is more clearly shown in figure 3d, where MOSFETs with InAs and InGaAs drain are compared, when V_{ov} (V_{gs}-V_t) is approximately -0.35 V. Evidently, the current increase with the InAs drain starts already at approximately 0.4 V, while with the InGaAs drain it starts after 0.7 V demonstrating a reduction in the tunneling current component as the Ga is introduced.

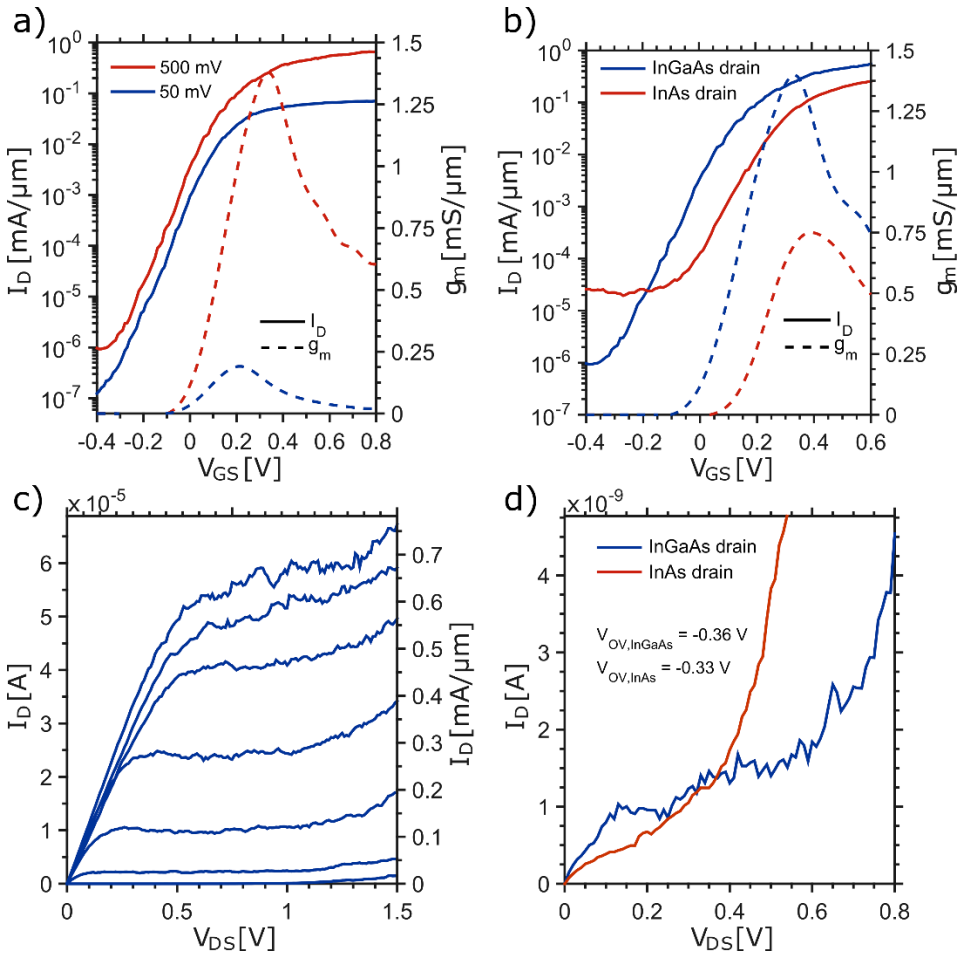

Figure 3. Transfer characteristics of MOSFET with InGaAs drain (a) showing high I_{on} and I_{off} < 1 nA/µm. The comparison of InAs and InGaAs drains (b) show clearly improved on- and off-state

performance with InGaAs drain. Output characteristics in (c) and (d) show improved saturation with InGaAs drain at higher biases due to reduced band-to-band tunneling and impact ionization.

To further investigate the leakage mechanism, transfer and output characteristics for the InAs/InGaAs MOSFET were measured at different temperatures (10, 60, 120, 160, 200, 240, and 295 K). The transfer characteristics in figure 4a show reduced minimum current levels at lower temperatures, which is attributed to a decreased tunneling rate caused by the increased band gap. Further, the data shows a V_T shift as a function of temperature, which can be explained by possible charge trapping either at the high-k interface or within the oxide. Similar effect is also detected in other III-V MOSFETs from our lab [22].

The output characteristics in figure 4b shows the off-state leakage current measured for different drain biases at V_{GS} = -0.5 V. To correlate the transport with the InGaAs band gap, the measured data is analyzed by fitting the data, using the least square method, to a formula describing tunneling through a triangular barrier [23]

$$I_{b2b} = A\frac{B}{\sqrt{E_G(T)}}\frac{V_D^2}{(1+V_D)\lambda}e^{-C\sqrt{E_G(T)^3}\left(\frac{(1+V_D)\lambda}{V_D}\right)},$$

$$B = \frac{\sqrt{2m_R^*}q^3}{8\pi^2\hbar^2},$$

$$C = \frac{4\sqrt{2m_R^*}}{3q\hbar},$$

where A is the cross-sectional area, E_G the band gap, m_R^* the reduced effective mass, and λ is fitting parameter describing tunneling length. The leakage current at 240 K (red line in figure 4c) was first fitted to define λ, which describe the tunneling length and therefore the electric field. From the fitting, λ =9.2 nm, therefore validating the model. To evaluate the leakage currents at

different temperatures, λ was kept constant and the E_G was varied. Notably, the estimated band gap values from this simple tunneling model does not match well with the empirical band gap model for InGaAs [24], as seen in figure 4c. Applying the detected V_t variation to the electric field of the model does not improve the matching either. Instead, the difference is attributed to the complex transport process in the transistor, where the tunneling carriers at the drain junction generate holes within the channel region. They may be injected to the source, recombine in the channel, or lower the barrier under the gate and cause thermionic emission of electrons, the so called bipolar effect. Hence, a more deliberate model is required. Notably, below room temperature, thermionic emission can be ruled out, as the leakage current is lower than predicted by the tunneling model.

In order to describe the transport processes, the model was modified by adding a temperature dependent function $y(T) = \frac{\lambda}{x(T)}$, where x(T) describes the temperature dependent hole escape rate related to the recombination and injection process at the source side. This is a simple modification to the model that describes the phenomena and provides a better matching. However, a more sophisticated model is needed in order to in detail describe the origin of the hole escape. The leakage current was fitted to the current equation

$$I'_{b2b}(T) = A\frac{B}{\sqrt{E_G(T)}}\frac{V_D^2}{(1+V_D)y(T)}e^{-C\sqrt{E_G(T)^3}\left(\frac{(1+V_D)\lambda}{V_D}\right)}.$$

Using this approach, the determined band gap follows the reported band gap for InGaAs reasonably well in the temperature range from 160 to 240 K. The leakage current seems thus to be mainly dependent on tunneling below room temperature, although at room temperature it seems necessary to include a current component related to thermionic emission to fully describe the transport.

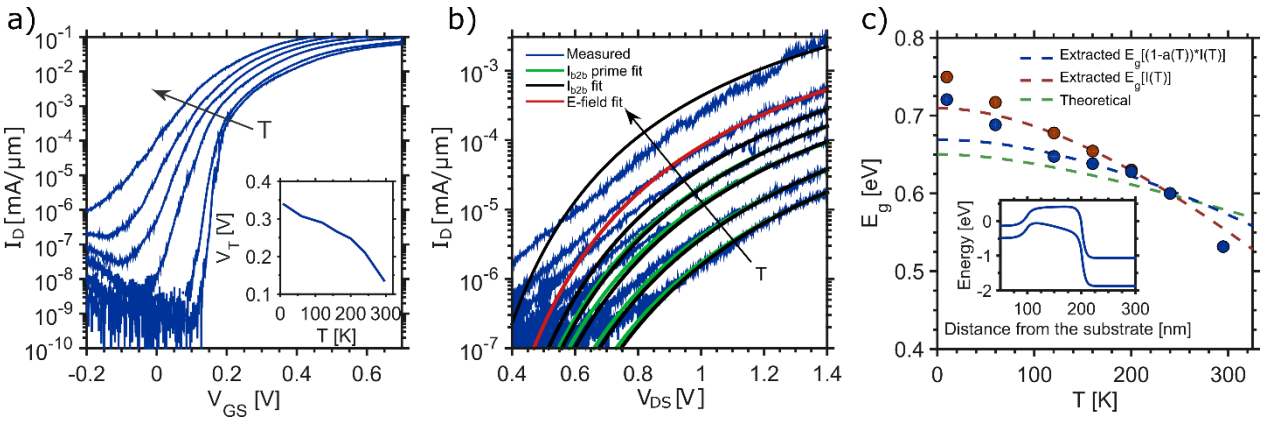

Figure 4. Transfer (a) and output (V_{GS} =-0.5 V) (b) characteristics measured at low temperatures (10, 60, 120, 160, 200, 240, and 295 K). Inset in (a) shows large V_T shift, which is attributed to carrier freeze out. Model describing tunneling through the triangular barrier allows a good fit for the leakage current (b) and shows that leakage current below room temperature is caused by band-to-band tunneling. Inset in (c) shows estimated band structure of an InAs/InGaAs MOSFET, when V_{GS} = -0.5 V and V_{DS} = 0.7 V, showing a small tunneling distance at the drain side.

In conclusion, we have shown state-of-the-art InAs/InGaAs vertical III-V nanowire MOSFETs on Si. The improved performance is mainly attributed to the introduction of wider band gap material ($In_{0.7}Ga_{0.3}As$) on the drain side, enabled by lateral strain relaxation of vertically grown nanowires. The approach has allowed us to decrease I_{off} below 1 nA/μm with improved breakdown voltage, which both are related to suppressed band-to-band tunneling and impact ionization. The devices show comparable or even advantageous on-performance as compared to vertical InAs MOSFETs, however the subthreshold performance is greatly improved, which provides a high drive current, $I_{on.}$ This approach opens a path to address not only high-performance applications but also Internet-of-Thigs applications that require low off-state current levels.

Methods

Nanowire growth. The nanowires were grown using metalorganic vapor phase epitaxy (MOVPE) in an Aixtron 200/4 reactor at a pressure of 100 mbar and a total flow of 13000 sccm.

After annealing in arsine (AsH_3) at 550°C, a 100-nm-long InAs segment was grown at 470°C for 50 s using trimethylindium (TMIn) and AsH_3 with a molar fraction of $X_{TMIn} = 3.0 \cdot 10^{-5}$ and $X_{AsH3} = 1.9 \cdot 10^{-4}$, respectively, corresponding to a V/III-ratio of 6.3. A 50-nm-long graded InGaAs segment was subsequently grown by adding Trimethylgallium (TMGa) and increasing its molar fraction from 0 to $X_{TMGa} = 4.3 \cdot 10^{-5}$ while reducing the TMIn molar fraction to $X_{TMIn} = 8.9 \cdot 10^{-6}$ during 20 s. The final vapor phase composition is In/(In+Ga)=0.17. After the graded segment a 300-nm-long n-doped InGaAs segment was grown for 55 s by adding triethyltin (TESn) at a molar fraction of $X_{TESn} = 1.6 \cdot 10^{-5}$ while the AsH_3 molar fraction was increased to $X_{AsH3} = 7.7 \cdot 10^{-4}$. The increased V/III-ratio for the top InGaAs segment resulted in a shorter diffusion length and the increased radial growth needed to provide low access resistance to the channel from the bottom source contact.

TEM analysis. The wires were transferred onto a copper TEM-grid covered by a lacy carbon film and analyzed in a JEM-3000F transmission electron microscope, operated at 300 kV in both conventional and scanning TEM (STEM) modes. High resolution TEM (HRTEM) micrographs were used for structural analysis while STEM in combination with EDX was used for elemental mapping and quantification along both the wire and of the seed particle.

Device fabrication. The transistor fabrication was started by spin coating the sample by a hydrogen silsesquioxane (HSQ) thin film. The HSQ was patterned by electron beam lithography (EBL), where the dose of the EBL defined the thickness of the HSQ layer. After developing the HSQ layer in 25% TMAH solution, 20 nm of W was sputtered and followed by a 3-nm-thick atomic layer deposited (ALD) TiN. The metal was anisotropically etched and the HSQ film was removed by HF leaving approximately a 10-nm-thick metal film only on the sidewalls of the nanowires.

A 50-nm-thick SiO_2 bottom spacer was deposited by plasma enhanced ALD. To remove SiO_2 from the sidewalls, thin S1813 resist mask was deposited and SiO_2 was etched by 1-100 HF. The bottom part of the nanowire was covered by the SiO_2 spacer and the top part by top-metal, therefore the gate region was locally etched forming a recess gate. In this particular case, the highly doped shell at the gate region was locally etched by digital etching, in other words repeatedly oxidizing the nanowire surface in O_3 and removing the oxide by HCl until the highly doped shell was removed. Based on our growth studies, the core diameter is a couple of nanometers larger than the gold particle diameter, therefore the nanowire diameter was inspected between the digital etching by SEM and the digital etching was stopped, when the diameter was less or same as the gold particle diameter. Next, 1 nm Al_2O_3 and 4 nm HfO_2 ALD high-*k* gate oxide was deposited and followed by sputtering of 60-nm-thick W gate metal. The device process was finished by defining a 300-nm-thick S1813 top spacer and contacts to the terminals. The final metal layer consists of 15 nm Ni, 30 nm W, and 180 nm Au.

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