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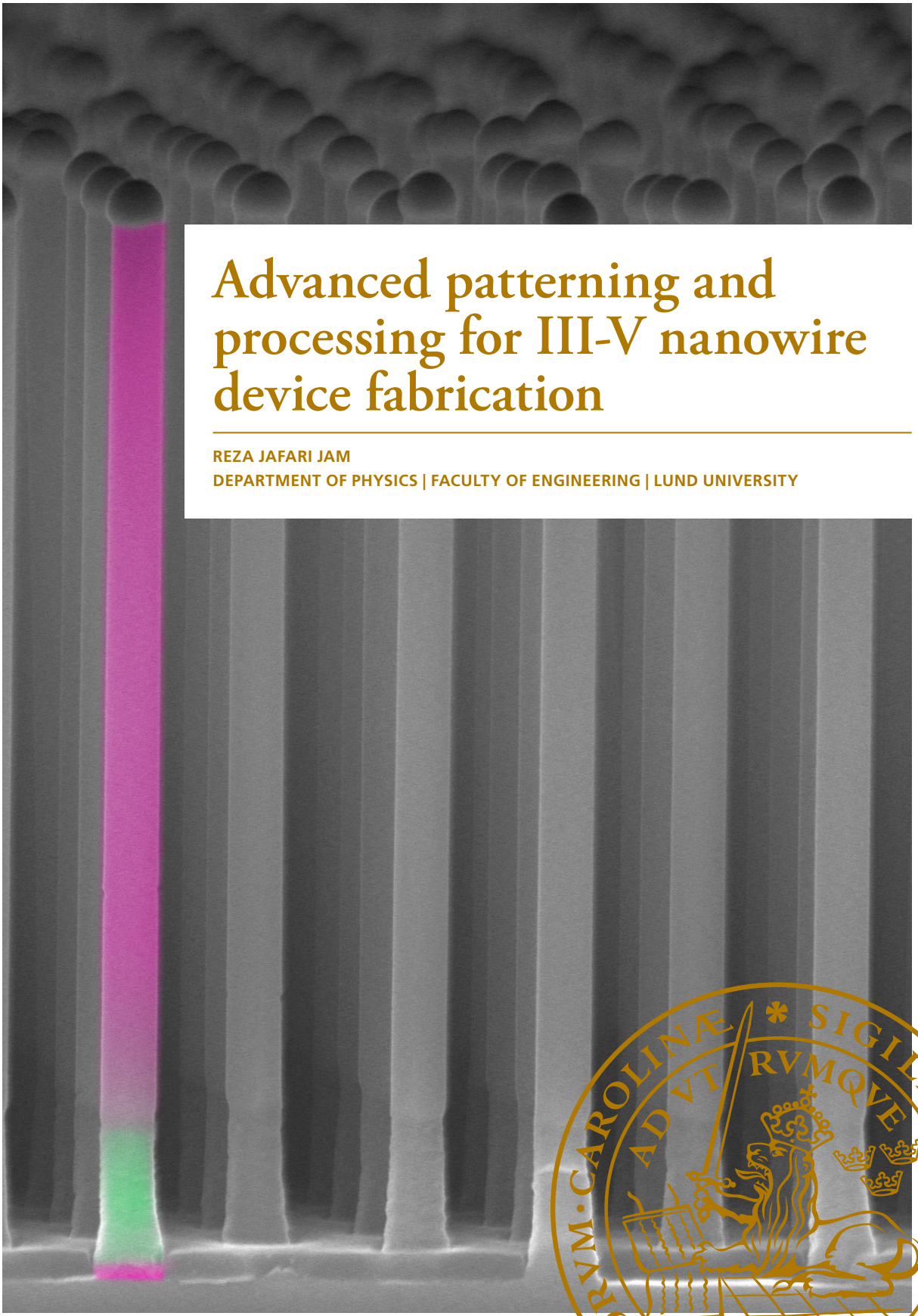

Advanced patterning and processing for III-V nanowire device fabrication

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Abstract

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In this work, we report on nanowire seed definition by gold electrodeposition. Electron microscopy inspection and optical spectroscopy confirm that the subsequently grown III-V nanowires have surface morphology and crystal quality comparable to those of nanowires grown from seed particles defined by conventional thermal evaporation. For seeding of substrates used in a typical growth run, we used around 650 times less gold compared to thermal evaporation.

We also demonstrated the possibility of depositing seed particles in deep holes etched in thick templates to facilitate template-assisted growth of nanowires on (001) Si and InP substrates. In addition to a functional p-n junction on an (001) InP substrate, the first reported InP-InAs-InP axial heterostructures on an (001) substrate was demonstrated.

In order to reuse the substrate for multiple growth runs, growth of AlAs-GaAs nanowires for epitaxial lift-off was realized. Using selective gold electrodeposition, we demonstrated deposition of seed particles on a substrate after nanowire peel-off. AlAs-GaAs nanowires were subsequently regrown demonstrating the potential of this novel technique for substrate reuse.

Key words

Nanowires, Template-assisted growth, Electrodeposition, Sacrifitial layer, Substrate reuse

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Cover photo: Cross-sectional SEM micrograph of a GaAs-AlAs-GaAs NW heterostructure which is used to facilitate substrate reuse. One of the NWs is artificially coloured to highlight the different materials along the NW.

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To the amazing women of my life, my mother and my wife

Content

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Fall 2019

Reza

Popular science summary

In everyday life, we often use electrical and optical devices such as sources of green energy like a solar cell, or a multi-functional communication apparatus like a smartphone. Such devices consist of several components, mainly fabricated from semiconductors. Silicon (Si) is by far the most used semiconductor for fabrication of electronic devices. Consequently, the corresponding industrial process lines are fine-tuned with respect to the detailed material properties of Si. However, Si alone cannot satisfy all the requirements of todays' electronics. With increasing use of e.g. cloud computing and storage, and the emerging internet of things (IoT) paradigm, disruptive optical solutions are a necessity for fabricating high-speed, low-power devices. Silicon is the perfect candidate for fabricating waveguides, couplers and other passive components, but it does not efficiently emit light and therefore cannot satisfy all the requirements for current integrated optical circuits. III-V semiconductors, e.g. indium phosphide (InP) and gallium arsenide (GaAs), are made from group III and group V elements in the periodic table. These compound semiconductors have excellent optical properties such as a strong emission and absorption of light in a suitable wavelength region, which makes them ideal candidates for active on-chip optical components like lasers and photodetectors.

Due to a large lattice mismatch, it is still a challenge to integrate III-V components with Si wafers. Although there are several approaches to realize III-V/Si integration, there is still plenty of room for new approaches. Semiconductor nanowires (NWs) are thin needle-like nanoscale building blocks with the potential to realize integration of optical and electrical devices on Si wafers. The small diameter of the NWs accommodates the strain caused by mismatch when growing them on Si. The strain relaxation offered in a NW geometry can also be used to integrate different III-V materials in a single NW, so called heterostructures, to create new artificial materials with tailored optoelectronic properties. Gold (Au) particles are well-known catalyst seeds for growing NWs. There are several methods to deposit these Au particles on a substrate, but none of them offers selective deposition on patterned substrates. This drawback significantly increases how much Au is wasted during fabrication and in some cases even makes it impossible to fabricate the desired NW device.

This thesis deals with development and applications of a novel Au electrodeposition method for growth and processing of III-V NWs. Gold electrodeposition is a method to selectively deposit Au on any conductive area, and thereby significantly reduce the wastage of Au deposited on unwanted areas. We showed that we could reduce Au consumption by a factor of 650 compared to conventional deposition methods such as evaporation, while growing large NW patterns without any loss in quality. One issue related to growth of NWs is that they tend to grow inclined relative to the surface of standard commercially-available (001)-oriented substrates, which makes subsequent device processing troublesome. A recently reported method, developed by researchers at IBM, proposed to grow the NWs in deep holes etched in a template, effectively forcing them

to grow vertically from the substrate surface. Gold electrodeposition is the only way to selectively deposit Au seed particles at the bottom of such deep holes. We have recently demonstrated the first successful guided growth of InP NWs, InAs/InP NW heterostructures and InP-based diodes in deep holes etched and Au-seeded in SiO_x templates fabricated on (001) Si and InP.

Nanowires have been shown to be excellent candidates for fabrication of high-efficiency solar cells. Gallium arsenide NW solar cells with an efficiency of 16.8% have recently been reported. In order to make them competitive with Si solar cells on a broad market, they need to become cheaper to make. The main part of the final cost comes from the usage of expensive III-V substrates and the patterning steps required to prepare the substrates for growth. Using our developed method for selective electrodeposition of Au seed particles, in combination with a novel concept of introducing a sacrificial dissolvable segment at the bottom of the NWs, we have proposed a new approach to reuse the expensive substrates and avoid repeating some of the complex patterning steps. After growth of large ensembles of GaAs NWs with an embedded AlAs segment, the NWs are embedded in a polymer and removed from the substrate by a simple peel-off technique. The embedded NWs can be used for flexible solar cells or be transferred to a cheaper Si substrate. During peel-off, the NWs break at the AlAs segment. The remaining stubs of AlAs on the parent substrate can be dissolved in a chemical solution to make the NW surfaces flat. Subsequently, a new round of Au electrodeposition prepares the substrate for regrowth of AlAs segments followed by the GaAs NWs. In this way, the substrate can be reused many times and the cost of the final solar cell thereby reduced by up to 100 times.

List of Papers

I. **R. J. Jam**, M. Heurlin, V. Jain, A. Kvennefors, M. Graczyk, I. Maximov, M. T. Borgström, H. Pettersson and L. Samuelson, "III−V Nanowire Synthesis by Use of Electrodeposited Gold Particles," *Nano Lett.,* vol. 15, p. 134–138, 2015.
I led the project and performed all the lithography steps and gold deposition prior to the growth. I was actively involved in analyzing the results and wrote the paper with input from co-authors.

II. **R. J. Jam,** A. R. Persson, E. Barrigón, M. Heurlin, I. Geijselaers, V. J. Gómez, O. Hultin, L. Samuelson, M. T. Borgström and H. Pettersson, "Template-assisted vapour-liquid-solid growth of InP nanowires on (001) InP and Si substrates", Nanoscale, 2019, DOI: 10.1039/c9nr08025b .
I led the project and performed all the lithography steps, gold electrodeposition and growth of the NWs. I was actively involved in analyzing the results and wrote the paper with input from co-authors.

III. **R. J. Jam,** Jason Beech, X. Zeng, Jonas Johansson, L. Samuelson, H. Pettersson and M. T. Borgström, "Embedded sacrificial AlAs segments in GaAs nanowires for substrate reuse", manuscript to be submitted.
I led the project and performed all the lithography steps, gold electrodeposition and growth of the NWs. I was actively involved in analyzing the results and wrote the manuscript with input from co-authors.

IV. V. J. Gómez, M. Graczyk, **R. J. Jam**, S. Lehmann, and I. Maximov, " Wafer-scale nanofabrication of sub-100 nm arrays by deep-UV displacement Talbot lithography", manuscript to be submitted.
I performed the gold electrodeposition and provided inputs on revised version of the manuscript.

Publications not included in this thesis:

V. V. Jain, M. Heurlin, E. Barrigón, L. Bosco, A. Nowzari, S. Shroff, V. Boix, M. Karimi, **R. J. Jam**, A. Berg, L. Samuelson, M. T. Borgström, F. Capasso and H. Pettersson, " InP/InAsP Nanowire-Based Spatially Separate Absorption and Multiplication Avalanche Photodetectors", *ACS Photonics* 2017, 4, 11, 2693-2698.

Abbreviations

AlAs	Aluminum arsenide
ALD	Atomic layer deposition
AsH_3	Arsine
BCB	Benzocyclobutene
C_4F_8	Octafluorocyclobutane
CF_4	Tetrafluoromethane
CHF_3	Fluoroform
Cl	Chlorine
Cr	Chromium
Cu	Copper
DC	Direct current
DEZn	Diethylzinc
EBL	Electron beam lithography
EDS	Electron Dispersive X-ray spectroscopy
GaAs	Gallium arsenide
GaInP	Gallium indium phosphide
GaP	Gallium phosphide
H_2S	Hydrogen sulfide
HBr	Hydrogen bromide
HCl	Hydrochloric acid
HRTEM	High-resolution transmission electron microscopy
ICP-RIE	Inductively-coupled plasma reactive ion etching
InAs	Indium arsenide
InP	Indium phosphide
IPS	Intermediate polymer stamp
LOR	Lift-off resist
MOVPE	Metal-organic vapor phase epitaxy
N_2O	Nitrous oxide
NH_3	Ammonia
NF_3	Nitrogen trifluoride
NIL	Nanoimprint lithography
NWs	Nanowires
O_2	Oxygen
PC	Pulse current
PECVD	Plasma enhanced chemical vapor deposition
PED	Pulse electrodeposition
PDMS	Polydimethylsiloxane

PL	Photoluminescence spectroscopy
PRC	Pulsed reverse current
RF	Radio frequency
RIE	Reactive ion etching
SEM	Scanning electron microscope
SF_6	Sulfur hexafluoride
Si	Silicon
SiH_4	Silane
SiN_x	Silicon nitride
SiO_x	Silicon suboxide
SiO_2	Silicon dioxide
STEM	Scanning transmission electron microscopy
TASE	Template-assisted selective area epitaxy
TA-VLS	Template-assisted vapor-liquid-solid
TEM	Transmission electron microscope
Ti	Titanium
TMAl	Trimethylaluminum
TMGa	Trimethylgallium
TMIn	Trimethylindium
UV	Ultraviolet
UV-LED	Ultraviolet light-emitting diode
VLS	vapor-liquid-solid
VSS	vapor-solid-solid
WZ	Wurtzite
ZB	Zincblende

Introduction

Semiconductor nanowires, NWs, have great potential as an emerging technology in electronics and photonics[1–8]. A leading technique used to grow semiconductor NWs is the vapor-liquid-solid (VLS) growth scheme in metal-organic vapor phase epitaxy (MOVPE).[9–12] Gold is the most commonly employed metal for the catalyst in this growth process, and a wide range of different NW-based devices have been fabricated using Au as a catalyst.[13–20]

There are several methods used to deposit Au, including aerosol techniques,[21,22] colloid particles[23] and thermal evaporation[24] but they all have some significant drawbacks when applied to controlled array deposition, deposition in high-aspect-ratio structures and re-deposition without excess lithography. When the technology for making highly efficient NW-based photovoltaics reaches its limits, it becomes increasingly important to reduce the fabrication cost by reusing the substrate. Substrate costs, lithography and Au consumption are all main components that determine the final cost of these solar cells. Cost reduction can be achieved by reusing the substrate in several growth runs, avoiding repeating lithography steps and using the optimum amount of Au in the process.

Electrodeposition has shown novel possibilities in nano-patterning with many important applications in semiconductor industry.[25–30] Gold electrodeposition facilitates selective Au deposition in arrays and high aspect ratio features.[28,31] Selective deposition helps when re-depositing Au and reusing the substrate without requiring additional lithography steps. The selectivity also significantly reduces Au consumption. Together, these lead to reduced material consumption and lower the cost of fabricating more complex structures. In addition, development of new deposition baths, particularly ones less toxic ones than cyanide baths, has made this process more environmentally friendly.

In 2008, Spurgeon et al. first demonstrated the use of Au electrodeposition for pillar growth.[32] They showed the possibility of reusing the substrate up to four times with a 10% reduction in the growth yield. In their work, however, the diameter of the pillars was in the range of micrometers, and the report did not present a detailed study of the electrodeposition process or the crystal quality of the grown material.

This work presents a detailed study of electrodeposition, and investigates the potential of Au electrodeposition for semiconductor NW seed definition. Chapter 1 introduces the electrodeposition technique, giving a review of direct (DC) and pulse electrodeposition (PED), as well as discussing different Au electrodeposition baths. In Chapter 2, Au electrodeposition on III-V and silicon substrates is discussed in detail. Chapter 3 deals with NW synthesis by the VLS method from electrodeposited Au seed particles.

Several growth examples are presented, along with an extensive discussion of the effect of key deposition parameters on the properties of the deposited material.[33] This chapter also reports on template-assisted VLS (TA-VLS) growth of NWs on (001)-oriented InP and Si substrates.

Finally, Chapter 4 discusses the deployment of electrodeposition for reuse of substrates in fabrication of solar cells. Gallium arsenide NWs with a sacrificial aluminum arsenide (AlAs) segment are grown from electrodeposited Au seeds. After a mechanical NW peel-off process, the remaining AlAs stub is etched away. Subsequent deposition of Au seeds and regrowth of GaAs/AlAs NWs demonstrates a successful reuse of these InP substrates. Chapter 5 summarizes the work and provides an outlook for future development.

1 Gold electrodeposition

1.1. Introduction

Electrodeposition was investigated from the very earliest years of modern electrical science, soon after the invention of the Voltaic battery in the early 1800s.[34,35] Together with copper (Cu), Au electrodeposition was the very first approach for surface metal coating. In addition to its color, Au has excellent material properties, such as corrosion resistance and high electrical conductivity, which make it suitable for a variety of applications. Gold electrodeposition was first applied to manufacture jewelry, but has expanded to other fields such as biomedicine and electronics.[28,36,37] In the third quarter of 2019, over 66 tons of Au were used in the electronics industry,[38] and it is estimated that more than 50% of it was deposited by electrodeposition for wire bonding, electrical contacts, connectors and switches.

This chapter reviews the basics of electrodeposition, and describes the components required to carry it out. Different types of electrodeposition are discussed, as is the role of the various bath components and the effects of sample condition. A comparison is given between two common types of Au solutions, cyanide and sulfite baths.

1.2. Direct current electrodeposition

At its most general, electrodeposition is the process of coating the surface of a metal with another metal by applying an electric potential. An electric current flows between a cathode – the substrate – and an anode. The electrical circuit is completed by placing the anode and cathode in a conductive solution, which contains ions of the material to be deposited. The anode may be made of the same metal as the material to be deposited, but this is not the case in this work.

There are methods to perform deposition from an Au complex without applying an electrical potential, using so-called electroless deposition, but they are beyond the scope of this thesis.[39–41]

Due to the applied current, the metal salt splits into ions. Positively charged metal ions, M^+, will travel to the cathode, the negative pole of electrochemical cell, and are reduced solid metal, eq. (1.1).

$$M^{n+}\,(aq) + ne^{-} \rightarrow M(\mathrm{s}) \qquad (1.1)$$

The deposited mass, m, follows Faraday's laws of electrolysis:

$$m = \left(\frac{\mathrm{QM}}{\mathrm{FZ}}\right) \qquad (1.2)$$

Where Q is the electrical charge in the bath, M is the molar mass, F is the Faraday number – the magnitude of electric charge per mole of electrons – and Z is the number of electrons transferred per ion. Considering that:

$$m = tAD \qquad (1.3) \quad \text{and}$$

$$Q = iT \qquad (1.4)$$

Where Here t is the deposited thickness, A is the deposition area, D is the density of deposited material, i is the applied current and T is the duration of applied current. From this, (1.2) becomes:

$$t = \left(\frac{\mathrm{iTM}}{\mathrm{ADFZ}}\right) = \left(\frac{\mathrm{JTM}}{\mathrm{DFZ}}\right), \qquad (1.5)$$

where J is the current density. Since all the other values are constants for a given material, the thickness of the deposited layer may be controlled by choosing a suitable current density and deposition time.

1.3. Choice of anode

The anode plays a crucial role in electrodeposition. Key anode parameters include the material from which it is made, and its dimensions. In some electrodeposition processes, the anode is made of the same material as the deposited coating. During such a process, the anode dissolves and replaces the material in the solution as it is used up in the coating. For example, the bath reactions in an alkaline Au cyanide bath with an Au anode are as follows:[42]

$$\text{Cathode: } [Au(CN)_2]^{-} + e^{-} \rightarrow Au + 2CN^{-} \qquad (1.6)$$

$$\text{Anode: } Au + 2CN^{-} \rightarrow [Au(CN)_2]^{-} + e^{-} \qquad (1.7)$$

A well-known problem is that so-called 'sludge' can affect the smoothness of the deposition. Sludge is made up of particles from the anode material, which are detached due to non-uniform corrosion. In order to avoid any contribution of sludge in the process one should put the anode in an anode bag, usually made of polypropylene. Using high purity anodes can also decrease the amount of sludge.[43] The anode can also be made of another material, which eliminates sludge formation and results in a more stable process. In this case, however, the solution must be replenished to compensate for material consumption. The anode and cathode reactions for an alkaline cyanide bath are:[42]

$$\text{Cathode: } 4[Au(CN)_2]^- + 4e^- \rightarrow 4Au + 8CN^- \quad (1.8)$$

$$\text{Anode: } H_2O \rightarrow O_2 + 4e^- + 4H^+ \quad (1.9)$$

$$\text{Full cell: } 4[Au(CN)_2]^- + 2H_2O \rightarrow 4Au + O_2 + 4H^+ + 8CN^- \quad (1.10)$$

For Au electrodeposition, platinized titanium (Ti) is the most commonly-used anode. Mesh anodes provide a better flow of solution, and hence a better uniformity of the deposit. The anode-to-cathode ratio, i.e. the ratio between the areas of the anode and cathode, is another important factor. At low anode-to-cathode ratio a higher rate of anode oxidation takes place, which is undesirable. It also affects solution depletion, which in turn affects deposition uniformity.

1.4. Electrodeposition baths

Cyanide is the most studied electrodeposition bath. However, because of health concerns, and the desired characteristics of the deposit, non-cyanide baths are used in many applications, especially in the electronics industry. In this section, we will review cyanide and non-cyanide Au solutions and discuss the advantages and disadvantages of each of them.

Cyanide baths

Cyanide baths are the most stable Au baths, but the presence of toxic HCN gas makes them less favored because of environmental and health concerns. Potassium and sodium salts are the most common form of cyanide complex. Potassium salts have a higher solubility. However, their very large negative reduction potential causes their cyanide baths to have a lower efficiency compared to others.[44]

Acid cyanide baths

Acid cyanide baths typically have a pH less than 5. Their low pH makes acid baths compatible with photoresists, which is important for the electronics industry. However, one should note that even at low pH, cyanide may still affect the photoresist.[45]

Acid cyanide baths have applications in industry for hard and bright Au deposition. Hard Au is the deposit alloyed with other metals to alter the deposit properties. Here it should be mentioned that low pH, or the use of additives such as hardeners or brighteners may increase the amount of carbon in the deposit. Research has shown that to decrease the amount of carbon, the bath temperature should be higher than 25 ˚C.[42]

Due to the lack of free cyanide in acid baths, Au cannot be oxidized from its metallic state, so anodes made of Au are not suitable, except when high current densities are used.

Alkaline cyanide baths

Working at a pH close to 10, alkaline solutions are not suitable for applications where resists and other polymers are involved. The Au deposits produced by this type of bath, which have a purity of more than 99.9%, are soft, and cannot be used where wear resistance is a concern. The excess of free cyanide in this bath does make it possible to use Au anodes, but may also affect the co-deposition of other metals because it alters their reduction potentials.

Neutral cyanide baths

With a pH between 5–8, and an absence of free cyanide, neutral baths are suitable for use with resists and polymers. At a pH greater than 5.5, the co-deposition of other metals is almost impeded, providing hard and soft Au deposits with a high purity.[42] Additives can be used to alter the physical properties of the deposit, making it hard or bright. With proper parameter selection, there is no need for additives in a neutral cyanide bath, so additive concentration does not have to be controlled, and the bath will have more current efficiency.[46]

Non-cyanide baths

Cyanide baths are good for Au electrodeposition in the electronics industry, because of the quality of the deposits and compatibility with photoresists, but there are health issues related to their high toxicity. Cyanide baths have a high stability, $\beta=10^{38}$, which means that in equilibrium, the electrolyte has a low tendency to oxidize at the anode or reduce at the cathode. Any alternative non-cyanide bath must exhibit a similarly high stability with a pH lower than 10.[28,42,44] Sulfites and thiosulfates are the most common compounds for non-cyanide baths. They have low stability, $\beta=10^{27}$, compared to cyanide baths, but they show acceptable deposit properties and good compatibility with most photoresists. However, it is not possible to deposit hard Au from these baths.[47]

Sulfite baths can produce deposits with good uniformity without effecting resists or polymers. They usually have a pH between 9–10 to retain compatibility for the microelectronics industry. Additives help to produce a more stable bath with a lower pH, but they can make waste disposal more difficult. For example, thallium acts as a grain refiner, but has toxicity issues of its own.[42]

1.5. Pulse electrodeposition

Electrodeposition may be carried out by applying a DC current between the anode and the cathode, as discussed above, or by applying a modulated current amplitude in PED.[48–52] Pulse current (PC) has an on time, T_{on}, followed by an off time, T_{off}. During T_{on}, the desired current density passes through the bath, while during T_{off}, no electrical current flows. Square-shaped pulses are often used because they provide a wide range of duty cycles and they do not need complicated pulse generators (see Figure 1.1). The duty cycle is defined as:

$$D = \frac{T_{on}}{T_{on}+T_{off}} \qquad (1.11)$$

Another important pulse parameter is the average current density, J_A, defined as the current density at which the deposition rate of PED and DC electrodeposition is the same. J_A, is defined as:

$$J_A = D \times J_P \qquad (1.12)$$

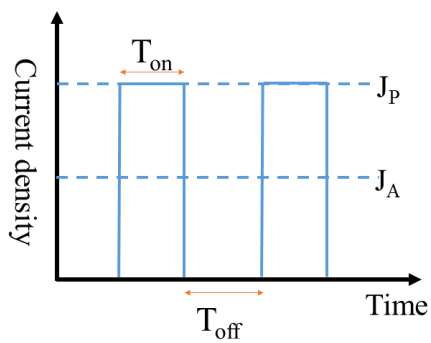

Figure 1. 1
Square pulse with basic parameters indicated

Where J_P is the peak current density. This means that for a pulse with a 20% duty cycle, the peak current should be 5 times higher than the DC level in order to have the same deposition rate as the DC electrodeposition.

Another important parameter for PED is the pulse frequency:

$$f = \frac{1}{\mathrm{T}} \qquad (1.13)$$

Where T is pulse period, $T_{on} + T_{off}$.

Due to the nature of the electrodeposition process, the solution and sample will form a capacitor at their interface, a so called Helmholtz double layer. The simple electrical circuit analogy comprises a resistor in the form of the electrode-solution interface connected in parallel to this capacitor.[53] This capacitor first needs to be fully charged for the current to reach the desired level for deposition and then at the end of the pulse the capacitor needs to be fully discharged.[54,55] Therefore, pulses with short rise and fall times, compared to the effective RC constant, lead to incomplete charging and discharging and non-optimal pulses. Figure 1.2 shows pulse shapes for a proper and improper choice of the on and off time, respectively.

The amount of ions reaching the cathode is governed by a diffusion layer close to the cathode which reduces the ion concentration during the on time. Figure 1.3 shows the simplified Nernst diffusion layer, indicating the ion concentration as a function of distance from the cathode. When the pulse is applied to the cell, the concentration of ions starts to decrease in the pulsating diffusion region (δ_p) until the pulse ends and the layer relaxes during the off time. The stationary diffusion layer (δ_s) extends to the bulk solution, and together with the pulsating diffusion layer form the entire diffusion layer. An applied pulse should be short to keep this diffusion layer as thin as possible but still long enough to fully charge the Helmholtz double layer.[55] One should not mix up the diffusion layer with the Helmholtz double layer, the former is usually several times wider than the latter and a matter of solution concentration rather than metal-to-solution interface.

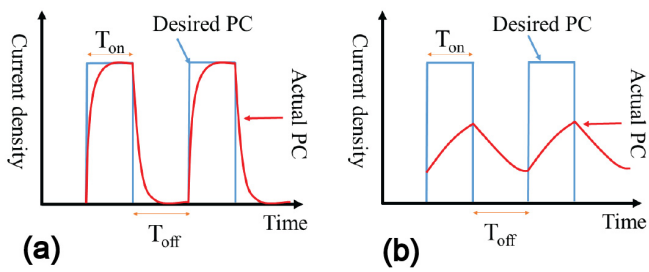

Figure 1. 2:
a) Pulses with long rise/fall times lead to a fully charged double layer and proper current pulse formation. b) Pulses with too short rise/fall times lead to incomplete charging/discharging and non-optimal pulse formation.

In addition, since the pulse duration is typically short – in the millisecond range – one can apply a significantly higher current density to the bath compared to DC electrodeposition. A higher current density increases the density of nucleation points which gives a better uniformity in the final deposit. The on time controls the size of the grains, so a short pulse facilitates a uniform deposit with less porosity and a finer grain size. However, finer grain size is not always achievable since it also depends on the details of the bath chemistry.[56] One drawback of PED compared to DC electrodeposition is the higher cost of the current generator.

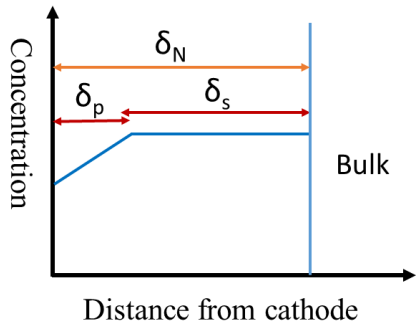

Figure 1. 3:
Schematics of Nernst diffusion layer. δN is the full length of the diffusion layer which is equal to the diffusion layer in DC electrodeposition.

Pulse reverse electrodeposition

Another type of PED utilizes a pulsed reverse current (PRC). There is no off time, instead two different current polarities are used: a cathodic current, J_C, and an anodic current, J_A, with durations of T_C and T_A, respectively. The average current density for during PRC is given by:

$$J_m = \frac{(J_C \times T_C)+(J_A \times T_A)}{T_C+T_A} \qquad (1.14)$$

PRC has advantages over PC. During the anodic time, not only is the double layer discharged, but any uneven part of deposit is etched away, providing a better uniformity. High frequency PRC eliminates the need for additives, which improves the physical properties of the deposit. It is also helpful when depositing alloys with varying composition. There are several studies claiming that PRC can improve uniformity in deposition of high aspect ratio features.[31,57,58]

1.6. Electrodeposition in the electronics industry

Electrodeposition offers several advantages for the electronics industry. It provides an economic way to deposit high quality material with the possibility to control various properties. Gold electrodeposition allows deposition of both soft and hard Au, which are required for high conductivity and hard wear resistance, respectively.[25,59]

In through-mask deposition, material is electrodeposited using a mask, such as the resists used in electronics fabrication. The desired pattern is transferred to the substrate using lithography, but there are some challenges related to electrodeposition. Material being deposited needs to find its way to the smallest features, so the wetting properties of the resist play an important role. Usually, resists do not have good wetting properties, so organic additives are added to the solution to improve this.[60] In addition, resists are sensitive to alkaline solutions, with a pH around 10, which can make it difficult to deposit materials with the desired properties.

Another difficulty is related to the uniformity of the deposit. The deposit may be non-uniform around a particular feature, for example, if edges experience a higher deposition rate. This can be reduced by using PED. A deposition pattern may consist of features with different dimensions or different densities of features, but for uniform deposits it is recommended to design patterns with an even distribution of features. The overall bath geometry also has to be taken into account, with auxiliary electrodes often added to avoid current crowding at the edges.[60,61]

Superfilling is a method to deposit void-free metal in high-aspect-ratio features.[62–65] The difference between through-mask electrodeposition and superfilling is that in the latter there is always a seed layer deposited to ensure better nucleation. In superfilling, various additives are added to the solution to increase the deposition rate at the bottom of the holes in the mask, and lower it at the top and on the sidewalls, so that a uniform deposit is formed.

2 Gold electrodeposition for III-V nanowire seed definition

2.1. Introduction

Gold is the most studied seed particle material for VLS growth of NWs.[10,66] Different methods of deposition have been used to define Au seed particles, all of which have their own drawbacks. While it is possible to generate small Au particles using aerosol technology, it is not possible to deposit them in an ordered array. Sputtering and evaporation can be used to deposit Au in lithographically-ordered arrays, but they cannot be used to deposit Au in high-aspect-ratio features, for example, when growing embedded NWs.

Metallization by evaporation and sputtering leads to significant amounts of material being wasted on the substrate and the sidewalls of the chamber. In thermal evaporation of thin films, around 1–2% of the evaporated material reaches the sample where the actual pattern usually covers only around 10–15% of substrate. This means that more than 98% of the material is wasted during the process. These methods also require low-pressure conditions, which makes them a low-throughput approach.

Gold electrodeposition, as a selective deposition approach, is a potential solution to all of these problems. It allows Au to be deposited in predefined places without any wasted material. Operation is under ambient conditions, making it a high-throughput approach. Electrodeposition will work with both organic resists, and inorganic masks (e.g. silicon dioxide (SiO_2) and silicon nitride (SiN_x)) if a suitable deposition bath is available. The use of inorganic masks facilitates reuse of the substrate, which is crucial for cost-efficient fabrication of many high-volume devices such as solar cells. There is no need for complicated process techniques to remove excess metal from the samples. Deposition in high-aspect-ratio structures for subsequent growth of complex embedded NW devices is also possible.

In this chapter, we will present our results on Au electrodeposition on Si and III-V substrates.

2.2. Gold baths

In this work, electrodeposition was carried out using a neutral cyanide bath, see section 1.4.1.3, with an Au purity of 99.9% (24K Pure Gold solution from Goldplating Inc.).[67] This bath has a pH of around 5.8, which is reasonably resist-compatible, although a certain degree of underplating does occur during the process as discussed in section 1.3. This solution also has a significantly lower price compared to electronics-compatible sulfite-based solutions. A platinized-titanium anode is suitable for this range of pH. About 950 ml of the solution is enough to coat a surface area of 8000 cm^2 to a thickness of 250 nm. For a reproducible process, the Au content in the solution should not decrease below 80% of the initial value without being replenished. The pH and bath temperature need to stay within 5% of their initial values. The pH can be adjusted by slowly adding 10% phosphoric acid to the bath.

The bath was heated to 35 ˚C to minimize carbon contamination, while retaining conditions as close as possible to ambient conditions. The purity of the deposited Au was examined by electron dispersive X-ray spectroscopy (EDS) and no traces of impurities were detected. The EDS in our transmission electron microscope (TEM) has a sensitivity of 1% so it cannot detect any signal if the concentration of the impurity is less than this.

2.3. Sample preparation

Plasma enhanced chemical vapor deposition (PECVD) and wet oxidation were used to provide the template on III-V substrates and Si, respectively. Nanoimprint lithography (NIL) and electron beam lithography (EBL) were used for patterning the resists, and the pattern was transferred to the underlying substrate with dry etching. In the following sections we briefly introduce each technique with its advantage and disadvantages.

Template deposition

PECVD was used to deposit the template (SiN_x and SiO_x) on III-V substrates while wet oxidation was used for growth of SiO_2 on Si substrates. Templates deposited with PECVD do not produce pure Si_3N_4 and SiO_2 so we use the sub-index x to donate the impurity of the deposit. Our technique usually results in a Si suboxide with Si deficiency.[68,69] This could have an effect on the growth as it might lead to vacancies on the template surface, causing unwanted growth on the template.

Nanoimprint lithography

NIL was performed using an intermediate polymer stamp (IPS) in a simultaneous thermal UV process from Obducat AB.[70] NIL is a high resolution, high throughput method for large-scale pattern transfer.[71] The pattern is created on a master nickel stamp, and then under specific conditions of pressure and temperature this stamp is pressed into a resist to generate the pattern on substrate. The technique has two main challenges. First, stamp and substrate separation can be difficult. Second, the stamp is affected by the process: stamps can break, and they may need to be cleaned or changed after a period of use, which adds cost to the process. To avoid this, it is possible to use the master stamp to fabricate an IPS replica. NIL is very sensitive, and it is hard to get the same results everywhere on the wafer. Even neighboring patterns may have different sizes due to imperfect processing or a defective stamp. This makes the subsequent electrodeposition and growth challenging. In this thesis the NIL resist is a negative epoxy resist of the TUx-xxx resist series in which UV light crosslinks the unpatterned parts, providing more stability for the unpatterned parts during the descum step where the remaining residues are removed by oxygen plasma etching.

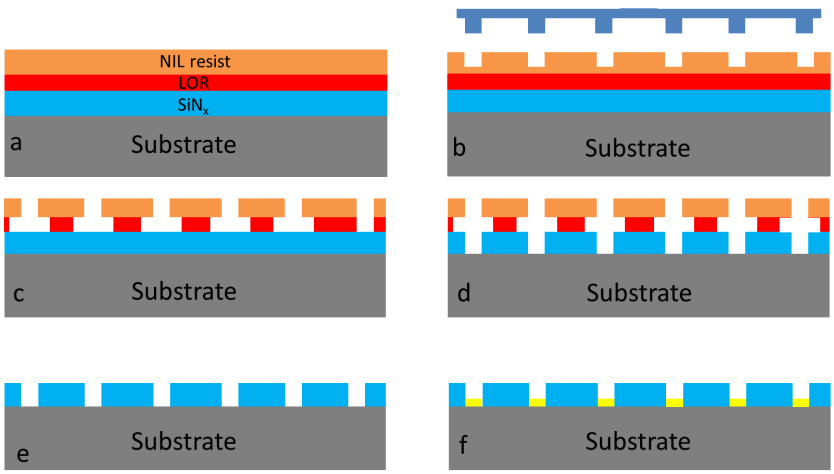

Figure 2. 1:
Different steps in a NIL process. a) The sample is spin coated with LOR and NIL resists. b) The pattern is transferred to the sample by pressing the stamp into the NIL resist. c) Sample after development and d) SiN_x etching. e) Sample after removal of resists. f) Final metallization step by Au electrodeposition.

Electron beam lithography

EBL uses electrons to change the properties of the resist and transfer high-resolution patterns to the substrate. High-energy electrons interact with electron-sensitive resist molecules, both at the resist surface and deeper inside. In a positive resist, the exposed

part is then removed by dissolving in a developer; while in a negative resist, the exposed part is retained, and the unexposed part dissolves.

The resolution of EBL is limited by the proximity effect, caused by forward scattering and back scattering of electrons. The electron energy is a crucial parameter. For thick resists, a high energy is required, as otherwise the electrons are more strongly scattered, making the features broader, especially towards the base. Challenges for EBL are to provide a good beam quality over long exposure times. Also, beam drifting and differences in sample height can change the focus, and hence beam quality. The low throughput of the EBL system is the main disadvantage of this technique. The lack of any need for a mask makes it highly favorable in terms of pattern design.

Dry etching

Wet etching results in isotropic profile, which means the material will be etched in all directions, lateral and vertical. In device fabrication most of the time, an anisotropic profile is desired. Reactive ion etching, RIE, is a physical-chemical dry etching technique which helps to achieve an anisotropic etch profile. In this, process gasses under low pressure are turned into ions and the ions are accelerated towards a plate that holds the sample and is negatively charged by a radio frequency (RF) generator. In order to have a better control over the etching, inductively-coupled plasma reactive ion etching (ICP-RIE) is available. ICP-RIE has an extra RF coil which makes it possible to control the density of ions and have a better control over the etching profile. Dry etching takes place not only due to bombardment of the sample with high speed ions – the physical etch – but also by chemical reactions between substrate and the process gases. Ion scattering, and the chemical nature of etching affect the anisotropic profile, leading to some degree of isotropic etching. To compensate for this the etch sidewall could be passivated by a polymer to reduce lateral etching. The passivation could be by switching between etch and passivation gases (Bosch process) or by simultaneous introduction of all gases (steady state process).[72–74] In the Si industry a cryogenic process is used to minimize the thickness of the passivation layer and increase selectivity towards the resist mask.[75,76]

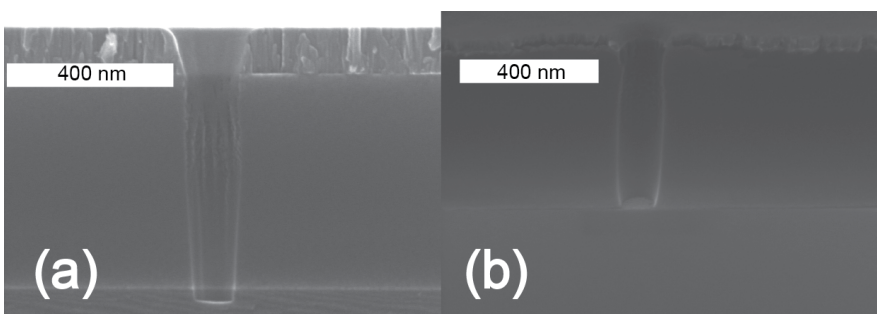

Figure 2. 2:
Etch profile of SiO_2 deposited on a) a Si substrate and b) an InP substrate. Evidently, the Si substrate is etched while the InP surface is left intact.

Dry etching of dielectrics

In this work, in order to etch the SiO_x and SiN_x, a fluorine-based recipe was used in which etching and passivation occur simultaneously. We used a CF_4 and CHF_3 gas mixture to etch SiN_x in a RIE system and a C_4F_8 and O_2 mix to etch SiO_x in an Oxford 100 ICP-RIE system. In deep etching of SiO_x, C_4F_8 acts as both etch and passivation gas while O_2 removes any redeposited carbon on the sample surface. The RF and ICP power were found to be important for deep etching of SiO_2. A high RF and ICP power is required to avoid RIE lag (low energy ions at the etch front) and to control sidewall passivation, respectively. These two parameters reduce the etch selectivity towards resist masks and a hard mask e.g. chromium (Cr) for deep etching is essential. As is evident from Figure 2.2, the recipe has a high selectivity to III-V substrate but a very low selectivity to Si. For Si substrates, over-etching should be avoided if it is necessary that the surface of the underlying substrate should remain unetched.

Dry etching of chromium:

In order to etch the hard Cr mask a standard chlorine based recipe is used. O_2 is very important in this process. If there is no O_2 in the reactor then the etch by-product is $CrCl_2$ which is volatile at around 1500 °C, way above the operation temperature of the ICP-RIE process. Adding O_2 to the process forms CrO_2Cl_2 as an etch by-product, which is volatile at room temperature. The trade-off is that O_2 is not desirable when a resist is used as the etch mask. Adding small amount of O_2 significantly improves the etch rate but above a 10% of gas mixture, O_2 degrades the etch rate.[77] The suitable value should be found for the equipment and the sample under test.

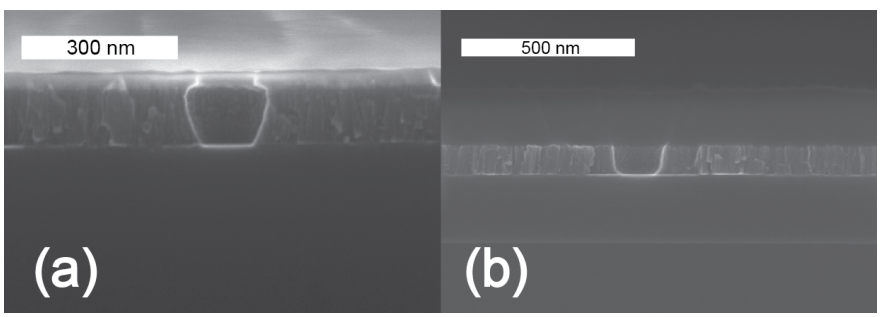

Figure 2. 3:
Etch profile of Cr a) using SiO_x as etch mask, b) e-beam resist as etch mask. the undercut does not occur with the e-beam resist. Etch masks are still in place.

A moderate RF power is required to etch Cr, we observed that the etch starts at RF power of 5 W and saturates at 20 W. The Cr etch rate is not significantly different in above mentioned window but the resist selectivity degrades significantly with increasing RF power. A RF power of 10 W was considered to be effective for a reasonable etch rate and selectivity. E-beam resist has a very low selectivity in the ICP-RIE system, which makes it hard to achieve deep etching with a resist mask. SiO_x or SiN_x have very

high selectivity in Cl-based recipe but in our experiments we always got an undercut in the profile which is not desirable, Figure 2.3. With the e-beam resist, the maximum etch depth was 85 nm but when a thicker template was needed, SiO_x was deposited by atomic layer deposition (ALD). For sub-100 nm holes we could not achieve etch rate more than 1 nm/min without use of ICP power unless we used a high RF power. However, high RF power reduces the selectivity more than ICP power. The story is different for trenches, where it is possible to etch sub-100 nm features without ICP power at a reasonable etch rate. It is well-known that trenches are etched faster due to higher transport of etch species and by-products into and out of the etch front. Although low pressure increases mask erosion, this process needs to be performed at low pressure: above 15 mTorr a keyhole profile was observed.

Substrate cleaning

Surface contamination can prevent material deposition or lead to poor adhesion, risking deposit peel off. Contamination can be extrinsic or intrinsic. Organic material or dust from the substrate are examples of extrinsic contamination, while native oxide is an example of intrinsic surface contamination.

Any resist residues from processing can lead to process failure. Silicon rapidly forms a native oxide when exposed to air, which makes it hard to electrodeposit high quality material on silicon. Organic residues can be removed by use of a solvent, but an aggressive cleaner, e.g. an acid, is required for the native oxide.

Acids such as HF will remove the native oxide, but the sample should be carefully rinsed afterward to remove any remaining acid, especially when using cyanide-based solutions. Electro-cleaning is another approach, where an electrochemical bath is used to clean the sample surface. Since the native oxide can form very rapidly, proper rinsing is important, and the choice of rinsing solution and environment is crucial. The rinsing solution should not facilitate oxide formation and it should not have any effect on bath properties.

Post deposition treatment is an important aspect, and simply rinsing in cold flowing water might not be enough to get rid of any residues from the solution. To achieve a cleaner surface, rinsing in hot water is suggested.

2.4. Deposition mechanism

Coherent material deposition may take place via a coalescence mechanism or a layer growth mechanism.[78] For Au electrodeposition, the deposition mechanism appears to be coalescence: the deposit starts by forming grains which then merge to form the final

deposit. The density and size of the grains are functions of applied current and deposition time respectively. To study the process mechanism, we interrupted a DC electrodeposition process on an n-type silicon substrate after a few seconds and inspected it by scanning electron microscope (SEM). As depicted in Figure 2.4 nuclei start by forming small grains which then merge to cover the whole surface. This confirms that a coalescence deposition mechanism occurs on the Si substrate.

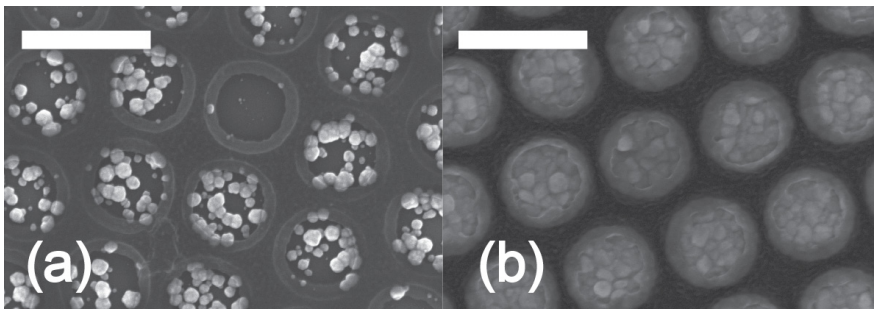

Figure 2. 4:
The process begins by forming grains after a few secs (a). These then merge to form the final deposited Au seed particles (b). Scale bar is 500 nm.

2.5. Electrodeposition on Si substrates

Silicon has always been the material of most interest to industry. There are several previous investigations of electrodeposition on silicon.[27,29,79] Huang et.al showed that grains will follow the surface property of the substrate for the first 50 nm, before becoming substrate-independent.[80] A clean and preferably intact surface is therefore needed for uniform and reproducible deposition. Here we present our results on electrodeposition on a Si substrate. Our substrate was highly n-doped, with a resistivity around 0.003 Ωcm.

Silicon forms a native oxide on its surface as soon as it is exposed to air, and this will affect electrodeposition. Since the process involves an interaction between the solution, the resist and the silicon surface, surface properties are important. There needs to be a high-quality hydrophilic surface with the proper wetting of profile sidewalls to permit the solution to pass through the holes in the mask and reach the Si surface.

Using EBL, a pattern of holes 100 nm in diameter and with a 1 μm pitch was transferred to a Si wafer. Our experiments showed that the wetting property of the resist plays an important role, and the smaller the desired features, the harder it is for material to reach the surface. Without proper wetting, not all holes are filled with the same amount of Au. The native oxide was removed in a mixture of HF:H_2O (1:100) for 2 min followed by rinsing in 99% ethanol for 5 min. Ethanol does not oxidize the surface of silicon, and it dramatically improved the yield from electrodeposition. We believe that ethanol led to

an improvement in the wetting properties. The sample was then placed in water, for less than 3 s, to remove any ethanol. The sample was subsequently mounted to the rack without drying to keep surface wetting at its best. Figure 2.5 shows the results. All holes are filled with a deposit of the same thickness. Using a commercial electro-cleaning and surface activator to achieve better surface properties would be a good way to obtain more stable deposition.

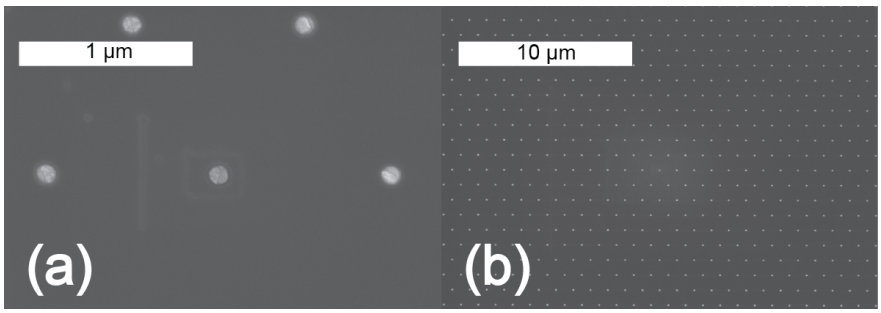

Figure 2. 5:
a) Deposited Au particles with good uniformity on a Si substrate and b) with high yield as compared to the pattern.

2.6. Electrodeposition on III-V substrates

Direct electrodeposition

Resistivity is an important factor in electrodeposition, and a low resistivity leads to a better deposit properties.[29] Doping level and resistivity are in direct relation to each other because high doping results in high conductivity (low resistivity), so p^+ and n^+ InP, GaAs, GaP wafers were used in this work. A *n*-type InP wafer with a doping level of around 5×10^{18} cm^{-c}, corresponds to a resistivity around $5\times10^{-}$ Ωcm. The difference in required current density for electrodeposition on different III-V substrates, regardless of feature size and doping type, comes from the difference in substrate conductivity.

Gold electrodeposition occurs selectively on conductive areas, hence there is no need to have a lift-off resist profile. However, TUx-xxx epoxy resists can leave some hard-to-remove residues on the substrate, making the surface less favorable for epitaxial processes. To avoid this, in the NIL process, we used a double layer resist profile consisting of a lift-off resist, LOR 0.7A, and a TUx-xxx NIL resist. The O_2 RIE process (descum) was continued until residues were removed from the pattern and the surface of the substrate was revealed.

A current density of 5.5 mA/cm^2 was applied to a *n*-type InP wafer with a doping level of around 5×10^{18} cm^{-c}. As is evident from Fig. 2.6a, the deposit forms a ring, with no

material deposited in the center of the opening. The reason is that sample was not conductive in the centers of the holes.

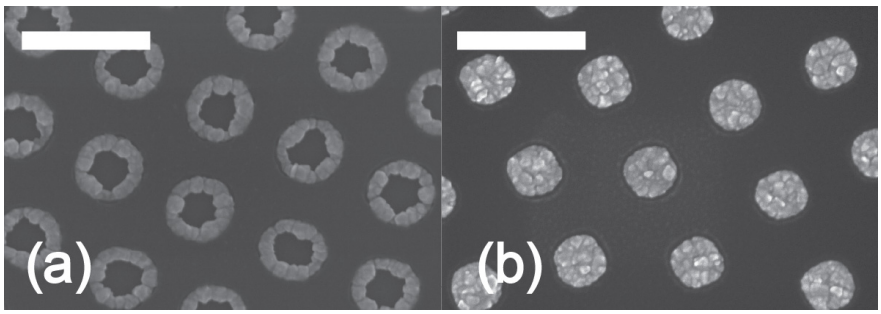

Figure 2. 6:
a) Deposition profile directly after descum and b) after HF cleaning. Resist mask is still in place. Scale bars are 500 nm.

The sample was placed in HF:H_2O (1:10) for 30 s and then the deposition process was repeated. Figure 2.6b shows the result: good deposits were observed across the whole sample. There are two possible explanations. Either the surface was oxidized during the descum process and this affected the center more than the edges, or the epi-ready oxide was removed at the edges but not at the center, where it blocked the deposition.

It is well known that a cyanide-based bath will gradually dissolve the resists and lead to under-plating. To avoid any under-plating a fast deposition process is required such that the sample is less exposed to the solution. We observed that for a PED process that lasts 250 s the under-plating is significant enough to affect the growth process. For process that involves a resist, in this case LOR 0.7, no under-plating was observed for a 10 s long direct plating.

Our measurements show that around 4.2 g of Au is needed to coat a 4-inch wafer to a thickness of 272 nm using a Pfeiffer Classic 500 evaporator, while the actual mass of Au on the final patterned substrate (with a pattern density of 6.25 holes/μm^2) is around 6.4 mg. Thus electrodeposition potentially provides a reduction in Au consumption by a factor of 650. The required mass of 4.2 g of Au in the evaporator is independent of wafer size, so it is clear that for smaller wafers and samples there will be an even greater reduction in material consumption. Even if it is possible to recover half of the Au from the evaporation chamber sidewalls, a 300-fold reduction is still achieved, which represents a significant cost reduction for a high-volume fabrication line.

Electrodeposition on p-type substrates

Free electrons are required for electrodeposition. This is not a problem for n-type substrates, but in p-type substrates charge is carried by an excess of holes. For electrodeposition on p-type substrates, usually a metallic seed layer is deposited by another deposition method, but this is not applicable in NW technology. In our setup, we use a set of

UV LEDs emitting at a wavelength of 405 nm to illuminate the substrate during processing and generate electrons (or rather, electron-hole pairs). Figure 2.7 below shows the result of the illumination on the electrodeposition. No deposition of Au is found in patterns without simultaneous light excitation.

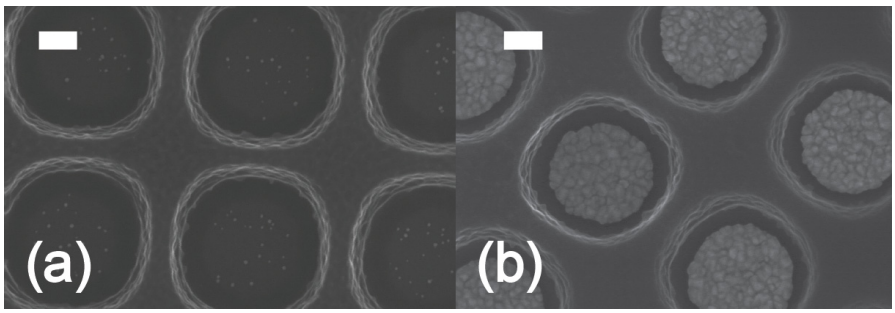

Figure 2. 7:
Deposition on p-type substrates, a) without IR illumination and b) with UV illumination. Scale bars are 100 nm.

Pulse electrodeposition on GaAs substrates

An n-type GaAs wafer was prepared to test the effect of PED on Au electrodeposition. As a reference, a peak current density of 5 mA/cm^2 was applied to the bath. To see the effect of the peak current on the properties of the deposit, current densities of 3 and 10 mA/cm2 were also used. As expected, the deposit thickness increased with the peak current density, as is shown in Figure 2.8.

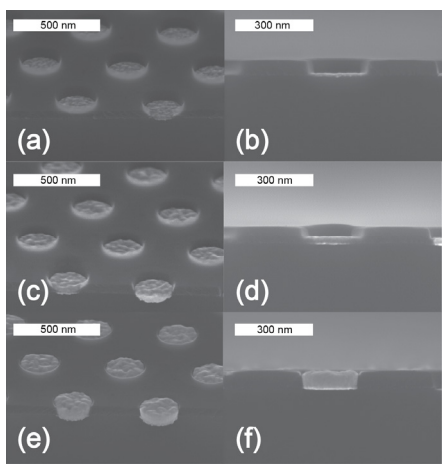

Figure 2. 8:
Effect of peak current density on deposit thickness using PED, a) & b) 3mA/cm^2, c) & d) 5mA/cm^2 and e) & f) 10 mA/cm^2.

Theoretically, we expect to have the same thickness for PED as for DC deposition if the same average current density is applied.[52] However, we observed a reduction in deposition rate from PED to DC deposition. To investigate this, we swept the pulse duty cycle. A longer duty cycle means more on time, and so a thicker deposit. Figure 2.9 depicts the effect of duty cycle on deposit thickness. Longer duty cycles do produce a thicker deposit, but the deposition rate reduces as the duty cycle increases. In these experiments, the pulse period was 50 ms with a peak current density of 5 mA/cm^2. For duty cycles of 10% and 20%, a 2-fold increase in deposition is expected, but the measured thickness increased by around 1.5 times. From 20% to 50% the factor is 1.25 and from 50% to 80% the factor is 1.2. The overall deposition time is constant, indicating a lower deposition rate as the duty cycle increases. The reduced deposition rate could be caused by charge build up at higher duty cycles, due to the longer on time. An on time less than 10 ms or an off time longer than 40 ms is optimum for this solution.

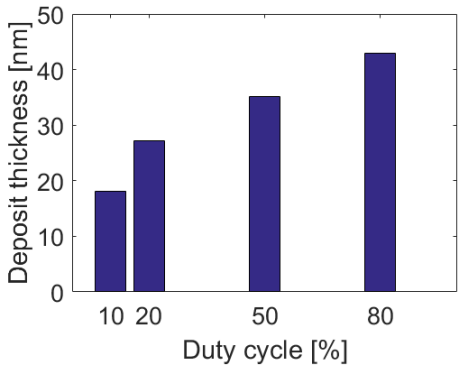

Figure 2. 9:
Effect of duty cycle on deposition rate at a frequency of 20 Hz. The deposition rate decreases as the duty cycle increases.

To study the effect of the pulse frequency, samples were coated using frequencies of 100 Hz and 1000 Hz. The current density does not change with frequency, so the thickness is not expected to change. However, the deposition rate seems to be reduced by increasing the frequency at a constant duty cycle. Following the discussion about the diffusion layer in section 1.5, this means that either the on time is very long so the pulsating diffusion layer extends far towards the bulk or the off time is not sufficient to relax the pulsating diffusion layer. However, surface roughness seems to be improved by pulsing. Higher frequency with the same duty cycle means lower on and off time times, and hence a smaller grain size, which could lead to a smoother surface.

Figure 2.10 shows measurements of the potential between the anode and cathode. It is clear that for the n-type GaAs polished on both sides, the pulse has a good shape, while for n-type Si polished on one side only, the pulse shape is distorted: it takes time for the pulse to reach its peak value and then a longer time to relax to zero. This is related to the capacitance at the cathode-solution interface (see section 1.5 on Helmholtz double

layer), in the case of silicon the capacitance is high so it takes almost the entire on and off time to charge and discharge it. We tried to investigate this by examining other Si substrates. We oxidized a wafer and then removed the backside oxide to create a smoother back contact, which improved the pulse shape and increased the measured potential.

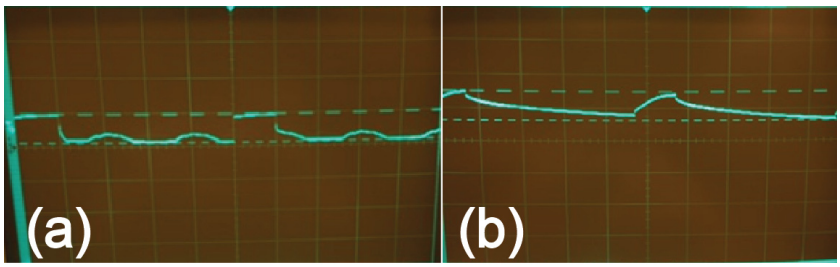

Figure 2. 10:
Actual pulse shape measured between the two electrodes. a) Double side-polished n-GaAs and b) one side polished Si.

A p-type GaAs wafer was prepared using NIL and light was shone on the sample during deposition. The deposition rate for p-type GaAs seems to be slower, despite the higher doping level than in the n-type samples. The measured voltage drop over the anode and cathode was lower, and the pulse shape showed the potential never reached its highest value. This explains the lower deposition rate. To obtain a thickness of 70 nm on a sample with an area equal to 1 cm^2, a current density of 5 mA/cm^2 was applied for 4300 cycles, as shown in Figure 2.11.

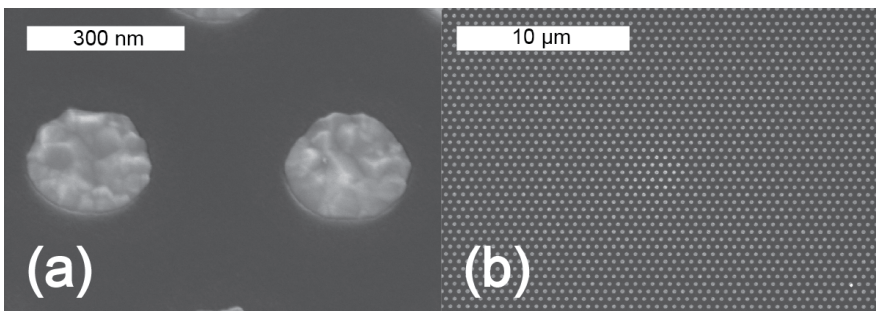

Figure 2. 11:
Electrodeposited Au particles on p-type GaAs. a) The deposit filled the 70 nm thick SiN_x template completely with b) a high deposition yield

2.7. Electrodeposition in high aspect ratio features

The challenge for through-hole plating is that material needs to penetrate the deep hole and reach the deposition site. A proper sidewall wetting is essential especially when dealing with sub 100 nm features. Etching polymer deposited on the sidewalls of the holes makes the wetting even worse. In case of Si it was easier to relax the wetting issue and achieve reasonable result. There are chemicals such as EKC 265 that can remove these polymers (Figure 2.12) and improve the cleaning of the native oxide. Rinsing in ethanol after HF dipping, improved the wetting properties even more. EKC 265 is incompatible with III-V substrates, making it hard to achieve a proper wetting and hence some degree of non-uniformity in deposit thickness was observed.

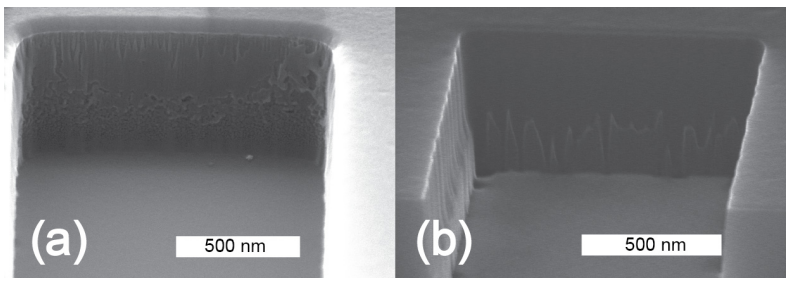

Figure 2. 12:
Effect of EKC 265 on removing the etch polymers. a) before and b) after using EKC 265. the polymers are significantely reduced.

We observed that a higher current density is required to deposit in deep holes compared to thicknesses below 150 nm. We also observed that the higher the aspect ratio, the higher the required current density. However, our results confirm that if the feature size is not in the sub-100 nm regime the aspect ratio dependency relaxes somewhat. This is because with larger feature sizes it is easier for the liquid to reach the deposition front. For sub-100 regime we have seen thickness variations among the deposited Au seeds between different holes and different samples, indicating that electrodeposition was not uniform and stable.

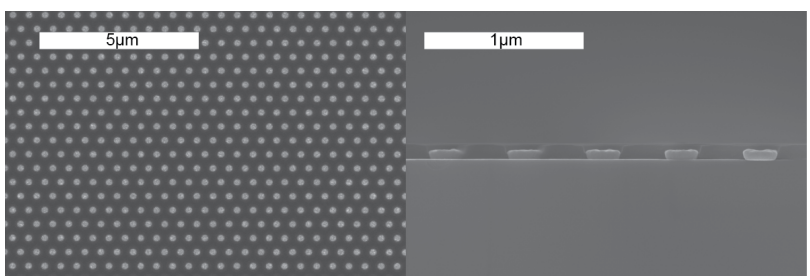

Figure 2. 13:
Electrodeposited Au on a 2-inch GaAs wafer, a) high yield and b) uniform deposit thickness.

2.8. Large scale electrodeposition

For deposition on larger, 2-inch wafers we used a deposition rack manufactured by Yamamoto-MS. When changing from a small bath to larger bath, it is important to take into account that the bath has a larger volume of material, 4 l, and the distance between the electrodes is different. As a result, a linear change in the current density is not sufficient to obtain the same deposit thickness. One needs to test and find the proper number of cycles as well. We observed that with the same current density as used for the small bath, we need almost half the number of cycles to achieve equal thicknesses. Deposition on 2-inch wafers was performed on samples prepared by NIL or Displacement Talbot lithography (Paper IV). Figure 2.13 shows our results for deposition on a 2-inch *p*-type GaAs wafer.

3 Nanowire synthesis

3.1. Introduction

There are many different techniques for nanowire synthesis, such as MOVPE, chemical beam epitaxy(CBE), and molecular beam epitaxy(MBE).[81–83] In this thesis we focus on NW growth using MOVPE. Possible growth modes include selective area (SA), VLS, and self-seeded growth; this thesis focuses on VLS.[84,85] In this chapter we will discuss NW growth using deposited seed particles on different substrates, together with morphological and optical characterization. Subsequently, we present TA-VLS growth of NWs on (001) substrates by using electrodeposition to define seed particles in deeply etched high-aspect-ratio features.

3.2. Vapor-Liquid-Solid growth mode

Particle-assisted VLS growth is the original and most well-studied technique for NW synthesis.[10,86] VLS uses a metal seed particle as catalyst to facilitate quasi one-dimensional NWs growth. The seed particle could be external, e.g. Au, or it could be self-seeding, as with In or Ga particles. External seed particles may be defined by various deposition methods, including electrodeposition.

Following deposition of the seed particles and removing any excess polymer, the substrate is moved to the growth reactor. The substrate is then heated to the desired growth temperature at which the effective pyrolysis of the metalorganic (MO) and halide precursors takes place. It has been asserted that the Au particle needs to be in the liquid state for growth to start, and so the growth temperature had to be above the eutectic temperature of the Au-substrate-vapor system. However, studies have confirmed that the seed particle does not need to be in the liquid state and the growth may be initiated in a vapor-solid-solid (VSS) mode provided that supersaturation at the seed particle is achieved.[87] However, the yield and growth rate are significantly affected under VSS as accommodation and precipitation in the liquid phase is considerably easier.[88]

When the particle becomes supersaturated as a consequence of providing growth species that alloy with it, the material begins to precipitate from the seed particle and if an overpressure of vapor precursors is maintained the NW starts to grow underneath the seed particle. As the growth continues, the growth species do not only reach the crystal from

the seed particle but will also react on the sidewalls as well. The growth is not purely unidirectional, but the growth rate on other facets is very low compared to the growth rate at the interface between the NW and its seed particle. Tapering due to lateral growth may occur, but can be impeded by introducing an etch gas such as hydrogen bromide (HBr) during growth.[89]

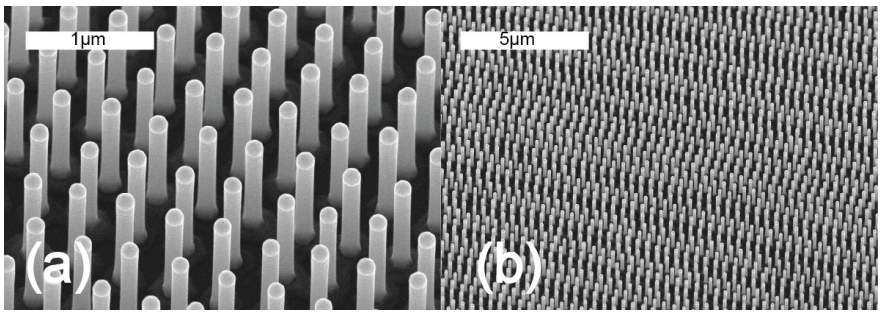

Figure 3. 1:
a) 30˚ tilted SEM image of InP NWs grown using electrodeposited Au particles indicating a good surface morphology. b) Low-magnification SEM image showing excellent growth yield with respect to the defined mask.

3.3. Nanowire growth by use of electrodeposited Au particles

Growth on InP substrates

InP NWs were grown using of 33 nm Au particles deposited by DC electrodeposition. Figure 3.1 shows NWs grown using electrodeposited Au particles. In order to compare electrodeposition with conventional thermal evaporation, samples with the same parameters were prepared using evaporated metal particles. The NWs grown using electrodeposited Au particles have good surface morphology, comparable with the evaporated sample. The electrodeposited sample also has a high growth yield with respect to the growth pattern density

Single NW photoluminescence spectroscopy (PL) was used to study the optical characteristics of the NWs. Low temperature PL, Figure 3.2, shows that the NWs grown from electrodeposited Au seeds exhibit a spectral redshift compared to NWs grown from evaporated Au seeds.

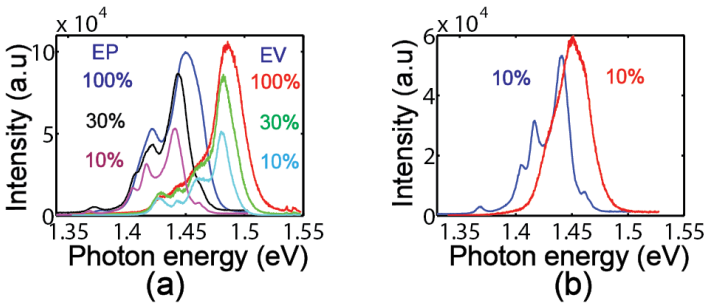

Figure 3. 2:
PL spectra of InP NWs for different laser intensities. a) Spectra for samples prepared with evaporation (EV) and electrodeposition (EP) using a resist mask and b) spectra for samples grown with (red) and without (blue) a SiN_x template.

TEM inspection shows that both NW samples consist of a polytype mixture of both zincblende (ZB) and wurtzite (WZ) crystal phases. High-resolution transmission electron microscopy (HRTEM) confirmed that NWs grown from evaporated seed particles show less crystal mixing compared to those prepared by electrodeposition, see Figure 3.3.

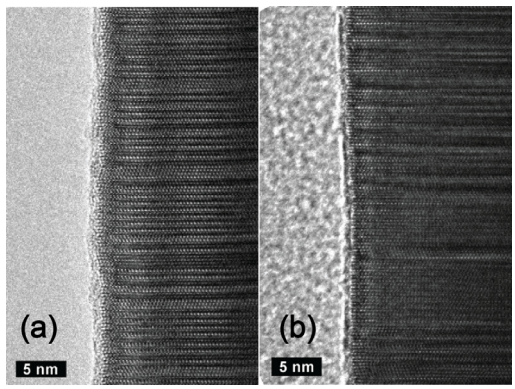

Figure 3. 3:
HRTEM images of InP NWs grown from a) electrodeposited Au and b) evaporated Au particles. Photo courtesy of Magnus Heurlin.

The differences in observed crystal quality could be a result of different conditions during growth. The temperature could have drifted in different places of the MOVPE reactor, or the gas flow could be different if the substrates are placed in different positions. Both these explanations are plausible since we grow the NWs on the two substrates in the same run. The different polytypism could also stem from differences in the Au seed volume and wetting angle during growth. It is clear that the electrodeposited Au particles are more porous, which means the volume of the final particle, after annealing, is different than expected. It has also been shown previously that the wetting angle of the

Au particle has a high impact on the crystal structure of the NWs.[90] It appears that post-evaporation Au thickness is not a good measure for comparison, but Au volume should allow reliable comparison.

Growth on GaAs substrates

Both *n* and *p*-type GaAs wafers were coated with different thickness of SiN_x as a growth template. Gold with thickness ranging from 25–75 nm was deposited by either DC electrodeposition or PED. Figure 3.4 shows a micrograph of NWs grown using 25 nm thick Au on an n-type GaAs substrate, where high yield and good surface morphology are achieved. Low temperature single NW PL measurement confirmed a mixed crystal structure for these NWs.

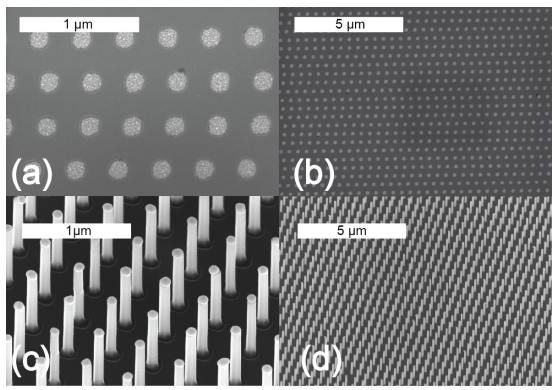

Figure 3. 4:
Top view of electrodeposited Au particles on an n-type GaAs substrate using a 25 nm thick SiN_x template. b) Zoomed out SEM image shows a good yield of the deposited particles with respect to the deposition template. c)&d) 30˚ tilted SEM images of GaAs NWs gr from electrodeposited Au particles at two different magnifications.

Eliminating parasitic growth

An undercut resist profile is usually used in order to facilitate metal lift-off in a lithographic process. The undercut is formed by using a double layer resist profile comprising a bottom lift-off resist, LOR, and the desired resist for lithography on top. The LOR is then partially removed by use of a developer to make an undercut. During the subsequent lift-off process, the remover will more easily reach the resist through the undercut and remove the excess metal. When evaporation is used for seed definition, there is a risk that small particles attach to the undercut. This problem is even more severe for nitride templates, since scattered ions will affect the undercut region during the template etching. The attached Au particles can, depending on growth conditions, cause some parasitic growth.

In order to eliminate this parasitic growth on GaAs substrate, Au electrodeposition was used. Figure 3.5 shows that the parasitic growth is completely eliminated by defining the Au seed particles with electrodeposition rather than by evaporation.

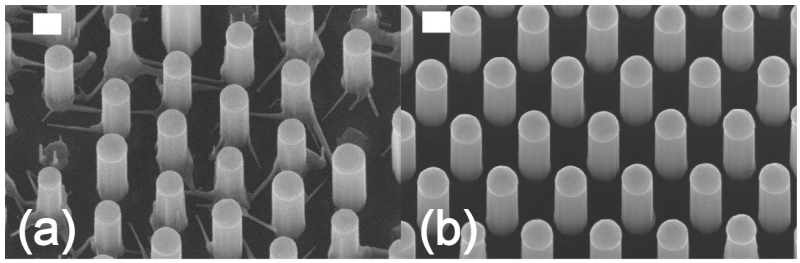

Figure 3. 5:
GaAs NWs grown from (a) evaporated seed particles and (b) electrodeposited seed particles. Parasitic growth is eliminated from the surface by using electrodeposited Au particles. Scale bars are 200 nm. Photo courtesy of Sebastian Lehmann.

Growth on GaP substrates

Hexagonal arrays of holes with 100 nm diameter and 1 μm pitch was transferred to a highly doped *p*-type GaP wafer coated with 30 nm SiN_x. Gold particles were defined using DC electrodeposition. The Au thickness was measured to be 30 nm, as shown in Figures 3.6a and 3.6b. Figures 3.6c and 3.6d show successfully grown GaInP NWs on this substrate. The yield was not extremely high compared to the number of dots defined by the pattern, which we attribute to the fact that the growth parameters were tuned for evaporated Au particles, which have a different Au volume compared to electrodeposited particles. However, we cannot eliminate the possibility this was related to defects in the lithography.

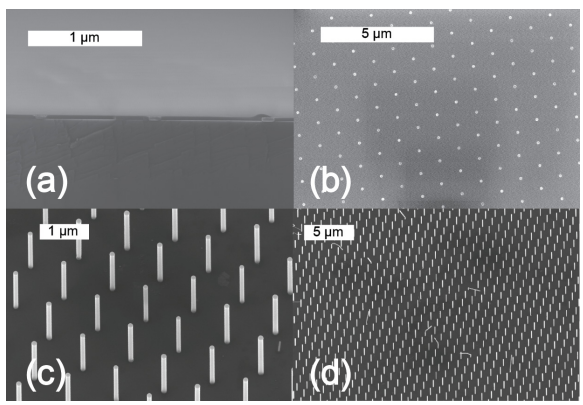

Figure 3. 6:
a) Cross section and b) top view of array of Au particles electrodeposited on p-type GaP. c) GaInP NWs grown from the seed particles shown in part a) & b). d) NWs were grown with a very good yield. Images in c &d are by courtesy of Alexander Berg.

3.4. Template-assisted VLS growth on (001) substrates

Growth of NWs on (001) substrates, for example, on industrial standard Si(001), is a major challenge. Nanowires tend to grow in the <111>B direction so they usually develop kinks if grown on (001) substrates.[86,91,92] Template-assisted selective area epitaxy (TASE) was used to grow InAs NWs on Si(001) substrates.[93,94] In this approach a thick growth template was used to guide the NWs so they grow vertically on (001) substrates. Because of the selective area growth mode, the natural challenge with TASE is that if the template material is crystalline e.g. Si, then parasitic growth and antiphase boundaries are inevitable. This limits application of TASE on SOI wafers because the growth could happen simply on top of the device layers.[95,96] Kum et.al used a two-step self-limited growth (TSSLG) mode to demonstrate defect free GaN NW based LEDs.[97] A self-seeding method was also used to grow nanospades in a template-assisted approach.[98] The main challenges with self-seeded mechanisms is that the seeding is random and the growth yield is very low and the growth need to be tuned.

Here we intend to develop an innovative technology to grow NWs on (001) substrates by VLS using a different template design. Using seed particles in NW growth can address the above-mentioned challenges, as the growth will only take place underneath the seed particle. Here we study template-assisted VLS(TA-VLS) using Au seeds to facilitate synthesis. With advances in alternative seed particles this approach could become compatible with mainstream Si platforms.[99–101] Challenges include etching the template, defining the seed particles, maintaining template quality, and then growing high-quality material on (001) InP and Si to form heterostructures. Inside the template the growth species can reach the growth front from the seed particle. This limits the growth scheme to the seed particle properties inside the template.

Definition and quality of template

For the InP substrate some parasitic growth on the template surface was observed while on the Si substrate the surface of the template was clean. Any vacancy on the sample surface can act as a nucleation site and cause parasitic growth. To investigate this issue in more detail, SiO_x deposition was conducted at different temperatures. It was observed that the template deposited at 100 °C had less parasitic growth compared to the template deposited at 200 °C, as is shown in Figures 3.7a&b. No traces of any material other than Si and O_2 was detected in EDS inspection of the template material. Due to the limits of the EDS technique, we cannot eliminate the possibility that the templates had other elements than Si and O_2 or that there may be a Si or O_2 deficiency in the deposit.

As is evident in Figure 3.7c, deposition of a thin SiN_x layer on top of the template can significantly reduce parasitic growth, but at the expense of different growth conditions. As the SiO_2 on a Si substrate is grown by wet oxidation, the deposit is considered to be

stoichiometric and, as is shown in Figure 3.7d, results in no parasitic growth on the template surface.

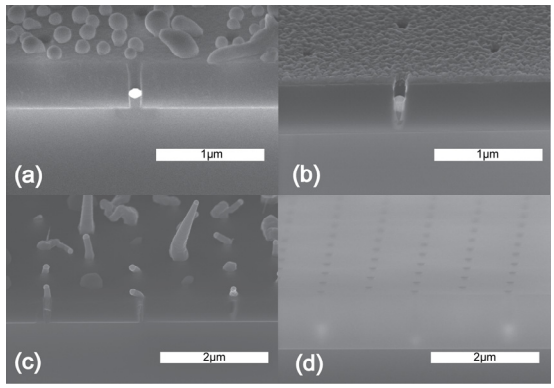

Figure 3. 7:
Effect of template quality on parasitic growth. a) SiO_x deposited at 100 °C, b) SiO_x deposited at 200 °C showed a higher amount of parasitic growth. c) A thin layer of SiN_x deposited at top of SiO_x improved the growth on the template surface. d) A stoichiometric SiO_2 template grown by wet oxidation on Si substrate completely eliminates surface growth.

Growth on InP substrates

In order to study TA-VLS growth of InP NWs in detail, a pattern with 100 nm openings on a 1 µm pitch was transferred to a wafer with a 500 nm thick template. Growth on an (001) substrate requires that the seed particle fills the template diameter to ensure that the NW starts growing with a size as large as the opening and does not kink and crawl on the sidewalls during growth. Our experiment results were in agreement with theory predicting that the Au thickness needs to be around 66% of the radius of the initial cylinder to form a hemisphere with the same diameter as the opening. Following this, 65 nm thick Au particles were defined at the bottom of holes. In order to feed the seed particle with In and initiate the growth, the reactor was flushed with In while the PH_3 supply was shut down. A high amount of parasitic growth on the sample surface was observed. EDS inspection confirmed that the material is InP. The presence of In hemispheres on the template surface can be an indication of In-seeded growth on the template surface. The high degree of parasitic growth, and the fact that the NW growth rate at the template surface is higher than the growth rate inside the template, clogged some of the openings and led to non-uniform growth over the sample. Thus flushing was avoided and the TMIn molar fraction was increased (lower V-III ratio). Although parasitic growth was not completely eliminated, it was significantly reduced while the growth rate under the seed particle was increased.

Growth inside the template is time-dependent which is expected as the diffusion of growth species to the growth front is faster as the embedded NW reaches the template opening. Due to the natural tendency of NWs to grow towards the <111>B direction it

is expected that NWs kink when they come out of template but surprisingly they were mostly vertical with some degree of tapering, Figure 3.8a. It was shown that fast growth of NWs can lead to fewer defects in the crystal.[102] This could explain the vertical growth of NWs when they emerge from the template. The growth rate outside the template is around 1 μm/min and the crystal has far fewer stacking faults compared to the part grown inside the template.

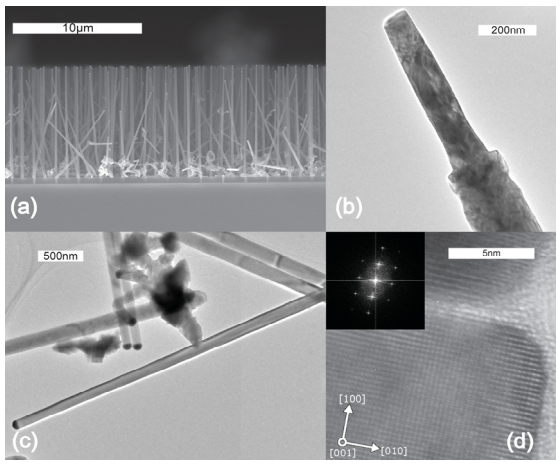

Figure 3. 8:
TA-VLS growth on InP substrates. a) 9 μm long InP NWs mostly grown vertical out of the template. b) TEM image of the NW part grown inside and c) outside of the template. The density of stacking faults reduced when grown out of the template. d) HRTEM of a NW close to the seed particle indicating a high quality ZB crystal. Inset shows the fft indicating a [001] crystal direction. Photos in part b-d are courtesy of Axel Persson

Despite the fact that unwanted growth on the template surface was inevitable, the grown NWs were shown to crystallize in the [001] direction, with a high density of stacking faults in the part grown inside the template, Figure 3.8 b-d. The difference in crystal quality in and outside of the template can be related to the fact that the NWs tend to grow towards the <111>B direction but the template is forcing them to grow vertically. Also, because the template profile has a positive slope, the Au particles diameter changes during growth which makes the growth mechanism unstable. As soon as NWs emerge from the template the Au particle becomes stable and govern the growth, resulting in a stable growth condition.

Growth with wider openings and a thicker template showed the same results, although the growth rate was higher due to faster diffusion in these holes. Figure 3.9 shows different SEM images of a substrate prepared for growth of 800 nm vertical NWs on a (001) InP substrate with an opening size of 250 nm, 500 nm pitch, and a template thickness of 1 μm. As of previous results, the InP NWs have a [001] crystal orientation with a high density of stacking faults along its axis.

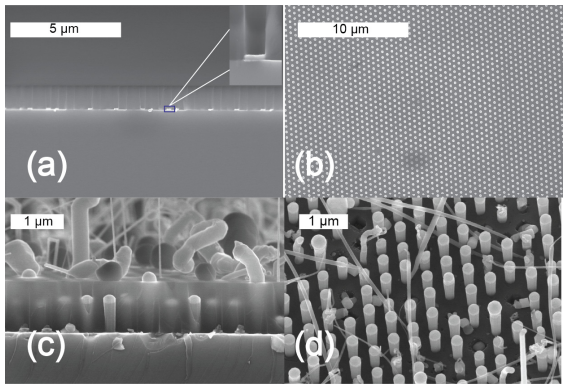

Figure 3. 9:
a) Gold deposition in deep via holes, b) Oxide template was removed to examine the deposition yield. c) InP NWs with 800 nm height were grown on a (001) InP substrate. d) Oxide was removed to check the morphology of the NWs.

Effect of dopants on TA-VLS

Introducing dopants to the reactor changes the growth scheme. First of all, the NWs do not grow vertically when they emerge from the template. This challenges the previous understanding that it might be rapid growth that led the NWs to grow vertically once out of the template.

In contrast to growth of free standing NWs, a high molar fraction of dopants did not degrade the growth yield inside the template. However, DEZn reduced the growth rate while H_2S increased it. To compensate for this the growth time for a *p*- segment was longer than *n* segment to obtain the desired length for each doping section. Using EBIC, a *p-n* junction was located inside the NWs, and the I-V curve showed a typical diode behavior with ideality factor of around η=2.6.

Growth of axial NW heterostructures using TA-VLS

Attempts to grow axial NW heterostuctures such as InP/InAs/InP failed when switching between desired group V precursors. Arsenic has a low vapor pressure and could react with any In particle trapped on the template surface instead of initiating NW growth inside the template. As an alternative, TMIn was shut down for a few seconds to deplete the Au particle from In. This led to growth of a pure InAs segment along the NWs, see Figure 3.10. The thickness of this segment was the same for a growth time of 20 and 60 s, which suggests that the amount of In in the particle reached the equilibrium value after about 20 s and the growth stopped. It would be interesting to study the dynamics of an Au particle at different states during this growth to investigate how it affects the growth conditions.

In conclusion, growth on InP substrates presents some challenges, including increasing the quality of the template and removing the Cr mask after deep etching. In addition, adhesion of oxide to the substrate is important: bad adhesion leads to delamination of

the oxide template during metal deposition. It would also be useful to study the doping profile of the NWs to help find their maximum possible doping level. This is an important concept as high doping of vertical NWs is still challenging and a requirement for electro-optical devices.

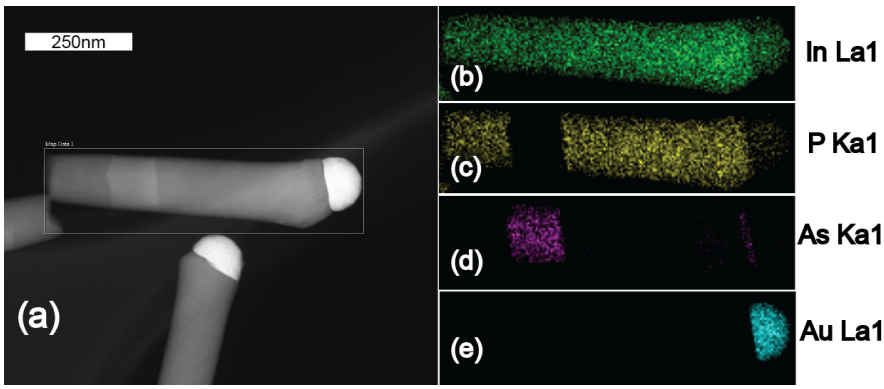

Figure 3. 10:
STEM/EDS image of a InP Nw with 100 nm embedded InAs segment. b-e colour code for In, P, As and Au, respectively. Photo courtesy of Axel Persson

Growth on Si substrates

1 µm thermal SiO_2 was grown on a n-type Si wafer in an oxidation furnace. A hexagonal pattern of holes with 100 nm diameters and a 1 µm pitch was transferred to the wafer. Si substrates are more challenging due to difficulties related to their native oxide. Also NWs need to have diameters of 100 nm, or less, to relax the lattice mismatch between Si and InP.

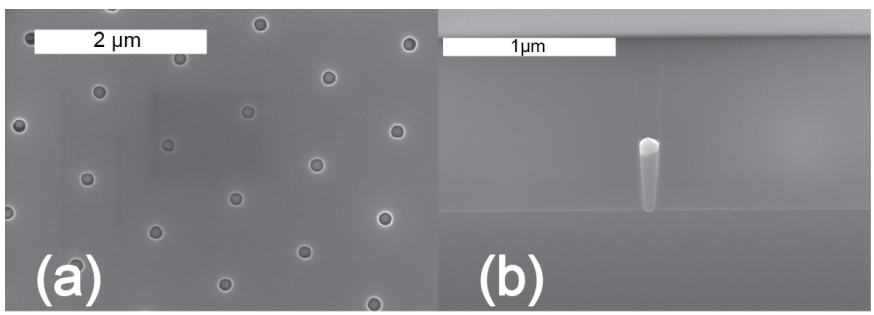

Figure 3. 11:
TA-VLS on 001 Si substrate. a) no parasitic growth on template surface. b) NW seems to be connected with substrate.

An important issue related to growth on Si is the formation of a native oxide on the Si surface. This oxide needs to be removed before growth to obtain a good interface between the grown material and the silicon substrate. Hydroflouric acid, HF, is a good candidate for this etching, but in this case it will etch the template as well, making the holes wider than desired. Studies have investigated how annealing at high temperature under AsH_3 overpressure can remove the native oxide.[103] Samples were annealed at 640–800 ˚C without and with an AsH_3 overpressure. Annealing at 800 ˚C under AsH_3 overpressure showed the best growth yield. As can be seen in Figure 3.11a, NWs are grown in all holes and there is no growth on the template surface. Room-temperature PL confirmed that the grown material is InP. HRTEM shows a ZB crystal structure with some diagonal twins. We do not yet understand why the crystal orientation is towards <111>; this could mean that the NWs do not have an epitaxial relation with the substrate. However, from Figure 3.11b it can be concluded that the growth indeed starts from the substrate surface.

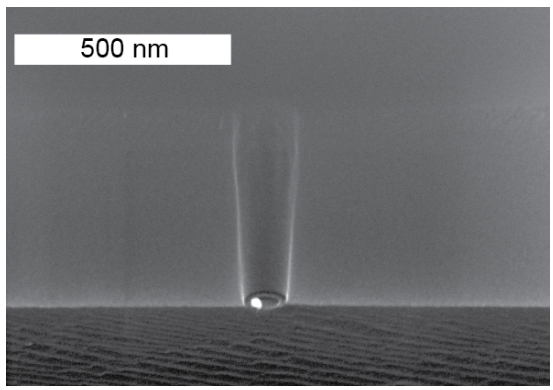

Figure 3. 12:
Profile of a dry-etched hole after an additional 5 minute HF wet etch. This wet etch process makes a step shape at the interface between the Si substrate and the SiO_2 which can act as a second source for nucleation of both Au deposition and NW growth.

A reason for the imperfect growth could be that the etching of the thick template could not be controlled precisely enough to stop exactly on top of the surface, resulting in a slightly damaged Si surface. Figure 3.12 shows what an imperfect surface could look like. Profiles like this can lead to a failure of the deposition, or provide different nucleation points for metal deposition and NW growth. For high-aspect-ratio features, etching is often not uniform at the bottom of holes. Thus, holes will have slightly different profiles and sizes, which affects the Au thickness. The etch could also be stopped at some point above the surface, before etching the rest of the hole profile with wet chemicals to provide an intact surface, albeit at the expense of a wider opening size.

Growth of heterostructures on Si

We have also grown NW heterostructures in which half the NW is InP and the other half is InAs. These NWs were examined by TEM as shown in Figures 3.13a-b and were shown to be ZB crystallized in the [001] direction with some diagonal twins. Interestingly, as shown in Figure 3.13c, no trace of P was detected and thus the NWs were pure InAs. The reason for this was not investigated in detail but it could be that the incubation time (time to reach supersaturation) is longer than the time needed for growth of the InP segment.

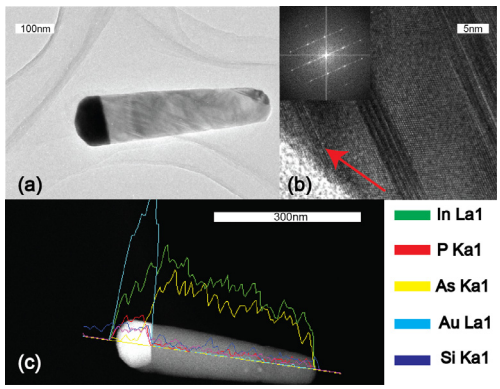

Figure 3. 13:
TEM image of InAs NWs grown on (001) Si using TA-VLS. a) TEM overview of the entire NW b) The NW crystal is ZB with a crystal orientation towards [001]. Diagonal defects are evident. c) No trace of P was observed in EDS inspection although the sample was supposed to be InP/InAs.

4 Substrate reuse

4.1. Introduction

As the theoretical limits of fabricating devices with higher fundamental efficiencies are reached, the focus has shifted more towards fabricating devices that have a low overall cost. In III-V solar cell technology, the substrate makes the largest contribution to the cost, followed by lithography. Reusing substrates while avoiding additional lithography steps is thus one of the most interesting and important current research fields in device fabrication.[32,104] One approach is to embed the grown material into a polymer and then peel them off from the growth substrate and transfer them to a cheaper substrate.

The peel-off process may be mechanical, in which the embedded NW-polymer composite is detached from the substrate by mechanical forces. This could lead to breaking of the polymer or the NWs, as well as leaving residues of the grown material behind, which would affect the next stage of growth. Epitaxial lift-off is another method, where a sacrificial layer of an easily removed material such as AlAs is grown first, and then the desired material is grown on top. The sacrificial layer is dissolved in an etchant, such as HF or HCl.[105,106] In this chapter we discuss application and challenges of implementing AlAs in NWs for substrate reuse.

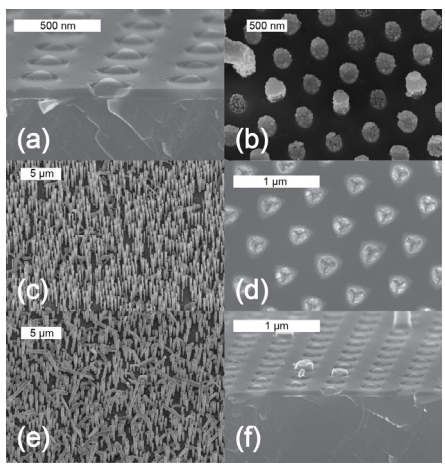

Figure 4. 1:
a) An InP substrate after peeling off the NWs. b) Electrodeposition of Au particles on sample shown in a). The remaining stubs are clearly visible. c) NWs grown on sample in b). d) Electrodeposition on a sample that was etched in HCl:H_2O (3:1). e) NWs grown on sample in d). f) Tilted cross-sectional SEM image of the

sample shown in e) after peel-off showing the remaining NWs in some part of the sample. Images in b)-d) are courtesy of Xulu Zheng.

Figure 4.1a shows a cross-section image of an InP substrate after mechanical lift-off. Figure 4.1b shows the reused substrate after electro-deposition of Au seed particles. Figure 4.1c shows the growth result, which does not have a satisfactory yield. This is because the substrate had some remaining stubs after the peel-off (Figure 4.1b). These stubs are longer than the template and cause the deposited Au to grow out of the SiN_x template and migrate across the surface during annealing and growth. Figure 4.1d shows an Au-deposited sample where the remaining stubs were etched with a mixture of $HCl:H_2O$ (3:2) for 20 s. The challenge here was to control the etch profile. The etch rate is very high, even for a very dilute mixture. This wet etch gives an isotropic profile and thus an etching of the material underneath the SiN_x template. The deposited Au then faces different barriers during growth, affecting the final growth property, as shown in Figure 4.1e. In addition, there are polymer residues after peel-off, and NWs remaining behind, seen in Figure 4.1.f. These affect both Au deposition and NW growth

The remaining polymer residues can be dissolved in a remover. The challenge is to etch away the remaining NW stubs without losing the template fidelity. As can be seen from Figure 4.1a, the stubs have oblique profiles, making them more challenging to etch uniformly at all points. It has been shown that during annealing, Au particles can dissolve some InP from the substrate.[71] It could therefore be useful to first deposit a thin layer of Au, and anneal it to erode the remaining stubs, and then deposit more Au to perform the growth. However, a precise control over the Au thickness and amount of group III during annealing is hard to achieve.

An alternative is to use a sacrificial layer for epitaxial lift-off. This section presents our results on application of AlAs NWs and Au electrodeposition for substrate reuse. The intention here is to grow a short AlAs NW and then grow the desired NW device on top. However, as has been shown before, growth of GaAs on AlAs is challenging and NWs will kink.[107]

4.2. Growth of GaAs/AlAs nanowires on GaAs substrates

In contrast to bulk epitaxial lift-off, a SiNx template is required to avoid excess lithographical steps. A 100 nm thick template was deposited on a p-type GaAs substrate using PECVD and was patterned by NIL. Seed particles were defined by use of thermal evaporation and lift-off. The properties of the SiNx template are very important. Adhesion to the substrate is a major problem, the template may delaminate at high temperature or be washed off under flowing water. This limits the growth temperature to an upper limit of 450 °C which is way below the reported growth for AlAs NWs in MOVPE and MBE.[107,108]

When the Au seed particles are Al rich (little to no Ga is accommodated) then they are in a solid phase and the process is VSS. This makes it challenging to start growth from the GaAs substrate, and in order to form a liquid particle, growth of a short GaAs nucleation stub was inevitable, see Figure 4.2a. AlAs NWs were grown on top of this stub, Figure 4.2.b.

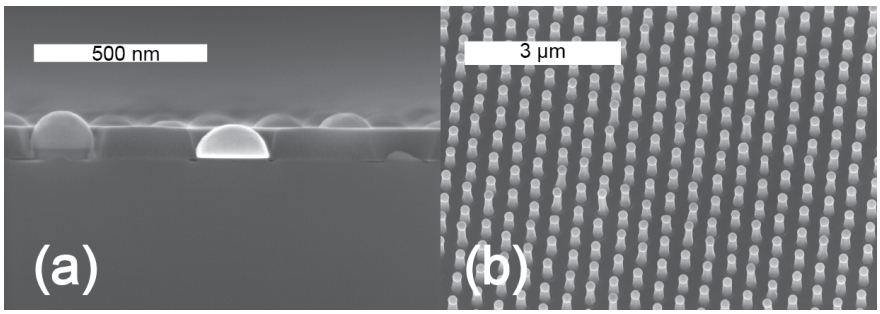

Figure 4. 2:
a) Growth profile after growing an GaAs stub. A difference in particle shape and hence wetting angle is evident. b) AlAs NWs are grown with high yield as compare to the growth template.

Although the growth had a reasonable yield, the growth rate was very low compared to e.g. GaAs. The growth rate is around 5 nm/min while GaAs is typically grown at a rate of about 150 nm/min. This difference could be either related to very low migration length of the Al species compared to Ga, or it could be that this process takes place in a VSS mode which has a significantly lower growth rate than VLS.[88] AlAs seems to grow quite fast in the lateral direction for a 600 nm long AlAs section, the measured diameter was 300 nm. HBr was employed to reduce lateral growth. HBr not only etch the lateral growth but it also improves particle stability, leading to a better growth yield.[89] As expected, HBr reduced the growth rate from 10 nm/min to 5 nm/min but sig-nificantly helped to increase the growth yield. However, a high amount of HBr can significantly reduce the growth rate of AlAs.

The central part of the sample had slightly lower growth yield compared to the edges. Changing the V/III ratio did not significantly improve this, it seems that a high V/III ratio was required which was not possible as the low TMAl molar frac-tion results in almost no growth of AlAs. As the yield was not significantly improved by different V/III ratio, we conclude that either the bad growth is due to a VSS growth mode, or more probably, the wetting properties of the particles are different as it is evident that some of the particles have a different wetting angle, Figure 4.2 a. The NIL stamp has some defects which can result in some deviation in profile of neighboring holes. This causes some of the openings to have different particle size and consequently have different wetting properties which leads to different growth conditions.

Finally, 2.5 µm long GaAs NWs were grown on top of an AlAs segment. The final growth yield is determined by the AlAs growth: where the AlAs has a high growth yield the final AlAs-Gas NWs were also grown with a high yield, as shown in Figure 4.3a.

Figure 4.3b is a cross section of the sample in which a contrast between the 500 nm AlAs segment and the 2.5 µm GaAs NW is evident. A shell growth of AlGaAs was observed in this step, to avoid it the HBr molar fraction was slightly increased to etch the shell away.

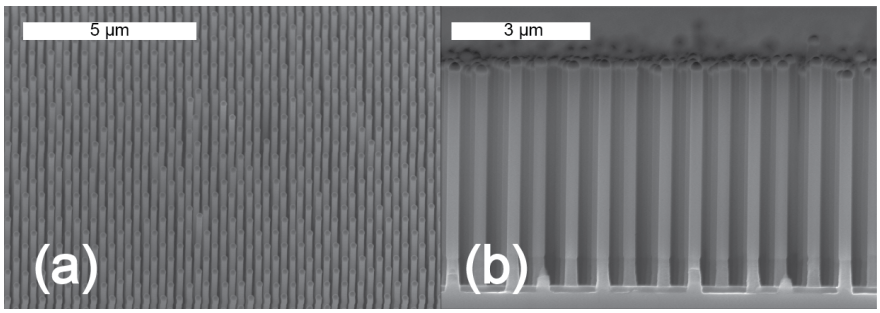

Figure 4. 3:
a) 30 degree tilted view of AlAs-GaAs axial NWs with high yield as compare to the patterned template. b) Cross-sectional SEM micrograph of the same sample showing the uniform growth. The contrast between AlAs and GaAs is clear.

4.3. Nanowire peel-off

In order to investigate epitaxial lift-off, the NWs were embedded in a double layer of LOR 0.7 and Benzocyclobutene (BCB). LOR acts as a sacrificial layer while BCB holds the GaAs NWs. A developer can remove the LOR and leave the NWs embedded in the upper BCB layer.

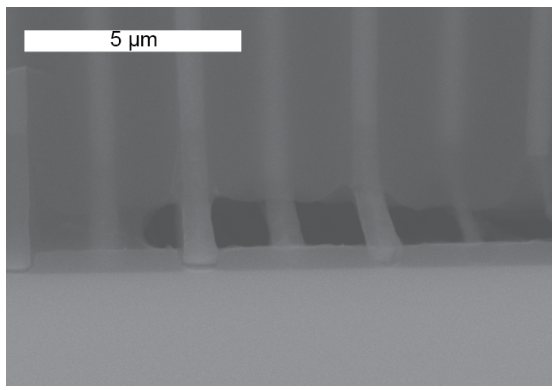

Figure 4. 4:
Status of a sample embedded in a double layer of BCB and LOR 0.7A. After 24 hours of development in MF319 just a few mm was removed.

This approach has an issue with that the penetration of developer into the pattern takes a long time and the developer can affect the template. Figure 4.4 shows a SEM image of a section close to the edge were the MF319 etched away the LOR. After 24 hours only a few millimeters were removed. A higher quality template could improve the low fidelity and provide a way to investigate epitaxial lift-off.

In this study the NWs were embedded in Polydimethylsiloxane (PDMS) and removed from the substrate. The sample was subsequently rinsed in Dynasolve 220 to remove any remaining PDMS residues.

4.4. Etching of sacrificial AlAs segment

The major challenge here is how to remove the AlAs. The most well-known etchant for this process is HF, but it would etch the SiN_x template very rapidly so an alternative $HCl:H_2O$ (1:1) solution was chosen. HCl etches GaAs (001) very slowly but it can etch the (111) substrates to some extent, to minimize this effect it was diluted with water.

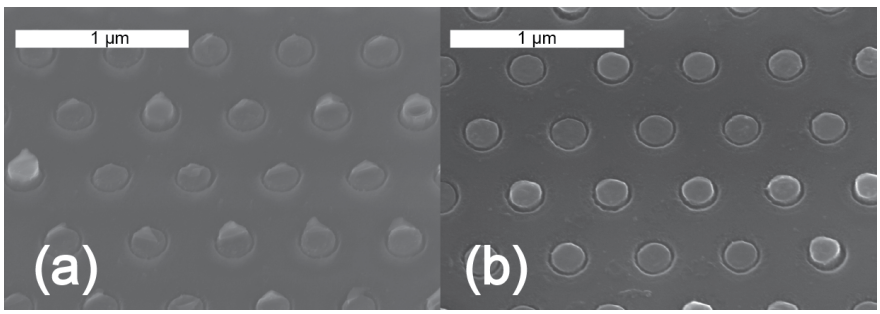

Figure 4. 5:
a) SEM image of a sample after peeling off the NWs. Residues from the AlAs are evident. b) After etching the AlAs away, all NW surfaces are flat and the template pattern is preserved.

Figure 4.5a shows the sample status after peel-off while Figure 4.5b shows the sample after etching the remaining AlAs segments away. Conventional peeling without a sacrificial layer will leave an oblique profile in the peeled NWs as well, which makes it challenging for subsequent device fabrication. An advantage of a sacrificial layer is that the bottom of the NWs after removing the AlAs is flat which is ideal for device fabrication.

4.5. Gold electrodeposition

In order to deposit the seed particles for regrowth electrodeposition was employed. The main challenge is the bottom GaAs stub; it does not completely fill the template opening so Au particles can position themselves anywhere on its surface. This makes regrowth challenging, and particles positioned on sidewalls could cause parasitic growth. Figure 4.6 shows the status after Au deposition; it is clear that due to deposition on sidewalls and underplating, the deposited Au is not enough to form a uniform deposit. As the Au solution cannot dissolve the SiN_x template, a reason for under-plating is that the template was not properly adhering to the underlying substrate and when it was placed in the solution it simply delaminated, allowing Au to find its way and underplate. A more careful observation in Figure 4.2a reveals that at the edge of the pattern the template is slightly delaminated, this could strengthen the above mentioned hypothesis. We strongly believe that this happened during the annealing at 450 °C.

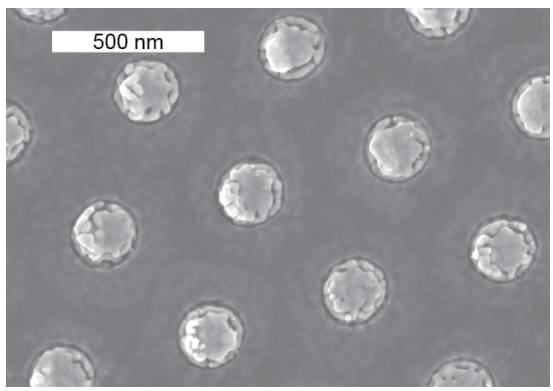

Figure 4. 6:
Sample after Au deposition for substrate reuse; underplating is evident.

4.6. Regrowth of AlAs/GaAs nanowires

As expected from the seed definition, the regrown material does not have a high yield. This is for two main reasons. First of all, the template was delaminated at some points. This happens because of the under-plating of Au and its movement underneath the template during annealing. This could be significantly improved by using a high quality template.

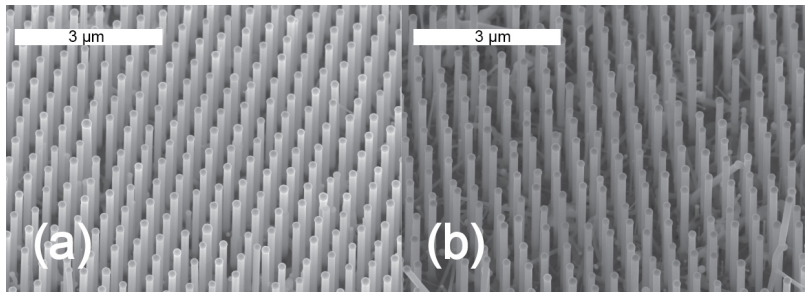

Figure 4. 7:
30 degree tilted SEM images of a) GaAs NWs and b) AlAs-GaAs NWs after regrowth. Pattern is preserved but the growth yield is affected by the under-plating and parasitic growth.

The second reason for low yield is deposition on the sidewalls of the GaAs stubs which can cause parasitic growth on the sample surface. However, the pattern is still preserved. Figure 4.7a shows the results of GaAs NW regrowth, the pattern is indeed preserved but parasitic growth on the surface is evident. Figure 4.7b shows the regrowth results for AlAs-GaAs NWs; as expected the yield is slightly lower as compared to the GaAs growth but still the pattern is preserved.

In conclusion the approach looks promising but there are challenges involved. The great achievement is that the template pattern fidelity is preserved after peeling off the NWs. Provided that the template has a good adhesion to the substrate, this means that the pattern fidelity could be preserved, making unlimited reuse a possibility. Since the template has a significant effect on all process steps the template quality and adhesion to the substrate both need to be significantly improved. The GaAs nucleation stub at the bottom seems to be a challenge. In the first instance, deposition on the sidewalls needs to be avoided. This could be improved by increasing the thickness of the Au particle so it fills the pattern completely. In order to fill the entire pattern, it might be possible to deposit the GaAs stub by electrodeposition.[109,110] On the other hand, the role of particles during growth depends on the amount of Ga it contains, so during regrowth the nucleation needs to start with Ga to grow the NWs. Maybe a better template allows for a higher growth temperature in which the growth mode is VLS, eliminating the need for GaAs nucleation stub.

5 Conclusions and Outlook

In this work, we have developed a selective Au electrodeposition technique for definition of seed particles in patterns for semiconductor NWs synthesis. Both organic resists and inorganic SiN_x and SiO_x masks were used to define patterns on silicon and III-V substrates. Gold was selectively electrodeposited from a neutral cyanide-based Au bath. In the case of p-type substrates, Au was electrodeposited by simultaneously illuminating the sample with light. Using electrodeposition, we demonstrated a 650 times reduction in material consumption with a significant improvement in throughput, as compare to thermal evaporation.

Pulse electrodeposition was implemented and shown to reduce the porosity of the deposited Au seeds. A smoother Au coating was achieved by using pulse electrodeposition rather than DC electrodeposition. The measured pulse shape, however, indicated issues with incomplete charging and discharging of the capacitor related to the electrode-solution interface, the main reason being a significant back contact resistance between the substrate and cathode holder.

III-V semiconductor NWs were grown on both n- and p-type substrates with characteristics and yield comparable with those grown from seed particles defined by thermal evaporation. From careful TEM inspection and PL measurements we cannot find any evidence of differences in quality of NWs grown from seeds deposited by electrodeposition and evaporation.

Moreover, we have developed TA-VLS to enable growth of InP NWs on (001) Si and InP substrates using a template. After electrodepositing Au seed particles at the substrate surface, vertical NWs were grown in the holes by MOVPE. The grown NWs have a [001] crystal direction with stacking faults. Using TA-VLS we also demonstrated guided growth of InP NW *p-n* junctions and axial InP-InAs-InP NW heterostructures. Further investigations of sample preparation are needed to improve the uniformity and reproducibility of the Au electrodeposition. In particular cleaning of the holes in the template is crucial for a successful growth of guided NWs with a high crystal quality and yield.

Finally, an AlAs sacrificial layer together with Au electrodeposition was employed for substrate reuse in fabrication of NW photovoltaics. After peeling off GaAs NWs comprising an AlAs segment from the substrate, the AlAs was dissolved in an etchant and Au seeds were deposited on short GaAs nucleation stubs on GaAs substrates. The subsequent regrowth of GaAs/AlAs NWs showed that the pattern is preserved. The yield, however, was not high mainly due to challenges involving the template properties.

The results of this work suggest that Au electrodeposition could be developed into a key resource in semiconductor NW technology with significant advantages compared to alternative deposition techniques such as evaporation.

For the next step TA-VLS on (001) Si needs to be investigated further. The clean surface of the template provides an easy process for contacting the NWs without requiring excessive lithography. From a lithography perspective, deep etching processes need to be investigated in more detail to achieve a more anisotropic profile as the lithography step seems to effect the crystal quality of the grown material. Etching must stop at the top of the substrate surface to keep it intact. A more detailed study on TA-VLS growth mechanism is also required to reduce the growth on the template surface for InP substrates. Different strategies need to be studied to improve surface wetting and uniform material diffusion into the deep trenches during electrodeposition.

Regarding the substrate reuse a higher quality template with reduced stress for better adhesion to the substrate is a necessity. A more detailed study of the growth mechanism would be helpful to understand what causes some of the AlAs NWs to crawl on the surface. The usage of PDMS is not cleanroom-compatible wherefore an epitaxial lift-off method could be a solution. Embedding NWs in a cleanroom compatible polymer and optimizing the solution penetration for faster penetration of etch species to the etch front is recommended in this case.

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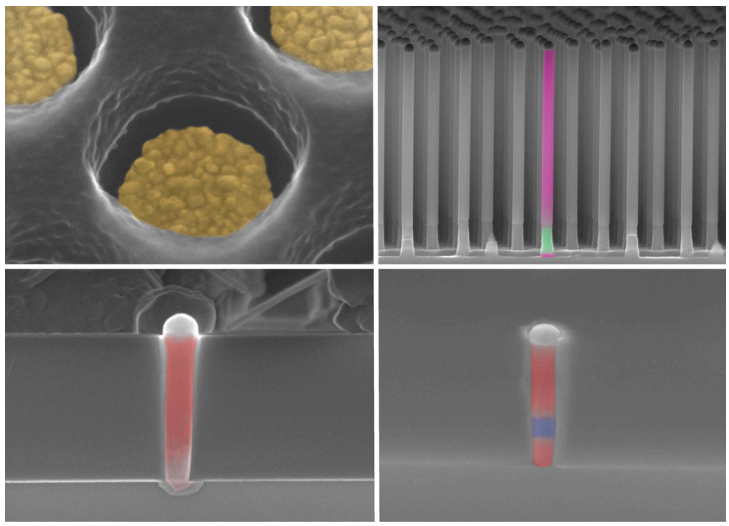

Advanced patterning and processing for III-V nanowire device fabrication

This thesis describes applications of gold (Au) electrodeposition in the synthesis of III-V semiconductor nanowires (NWs) and related devices. We have shown that Au electrodeposition can successfully replace conventional methods of seed deposition such as thermal evaporation.

The top left image in the figure shows an SEM micrograph of Au seed particles defined on a p-type InP substrate using a resist as the deposition mask. The Au particles are coloured artificially. **The top right image** is a cross-sectional SEM micrograph of a GaAs-AlAs-GaAs NW heterostructure which is used to facilitate substrate reuse. One of the NWs is artificially coloured to highlight the different materials along the NW.

The bottom left image is a cross-sectional SEM micrograph of a NW p-n junction grown on a p-type (001) InP substrate using TA-VLS. This approach is promising for integration of NWs with the (001) substrates used in mainstream industry. The p and n sections are artificially coloured in different shades of red. **The bottom right image** is a cross-sectional SEM micrograph of an InP-InAs-InP NW heterostructure grown by TA-VLS on a p-type (001) InP substrate. The estimated position for the InAs segment, as confirmed by STEM, is artificially coloured in blue.

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