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Gate-Length Dependence of Vertical GaSb Nanowire p-MOSFETs on Si

Adam Jönsson, Johannes Svensson, Erik Lind and Lars-Erik Wernersson

***Abstract*— The effect of gate-length variation on key transistor metrics for vertical nanowire p-type GaSb MOSFETs are demonstrated using a gate-last process. The new fabrication method enables short gate-lengths (L_g=40 nm) and allows for selective digital etching of the channel region. Extraction of material properties as well as contact resistance are obtained by systematically varying the gate-length. The fabricated transistors show excellent modulation properties with a maximum I_{on}/I_{off} = 700 (V_{GS} = -0.5 V) as well as peak transconductance of 50 µS/µm with a linear subthreshold swing of 224 mV/dec.**

***Index Terms*—Vertical, nanowire, III-V, MOSFET, GaSb, scaling**

I. Introduction

METAL-OXIDE-SEMICONDUCTOR Field-Effect Transistors (MOSFETs) based on III-V channel materials integrated on Si, have proven to be viable technology booster for n-type digital and radio frequency (RF) devices [1]–[3]. Antimonide (Sb) compounds such as GaSb and InGaSb are promising alternatives for III-V p-channel MOSFETs, due to high bulk hole mobility [4]. The material is also an essential part of InAs/InGaAsSb Tunnel-FETs [5]. However, certain process modules, like gate-stacks and ohmic contacts, for the GaSb MOSFETs are not as optimized as for corresponding n-type MOSFETs, which limits the transistor performance [6]–[8]. Strong p-type MOSFETs based on III-V material is essential for future logic implementation and their integration with state-of-the-art n-type RF transistors. Combinations of more conventional p-type SiGe channel devices integrated with n-type III-V InGaAs based devices has been proposed [9], [10]. However, material selectivity during processing may limit this type of material integration, which motivates further studies and development of III-V based p-type transistors.

To circumvent issues, such as various short channel effects due to deteriorated electrostatics, concerning continued transistor scaling alternative geometries are critical [11]. Gate-all-around (GAA) geometry using vertical nanowires is one option with a projected benefit at the 5 nm node [12].

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A vertical nanowire geometry also provides decoupled gate length and contact geometry with regards to footprint area [13]. However, vertical geometries require novel lithography methods to substitute conventional fabrication techniques [14].

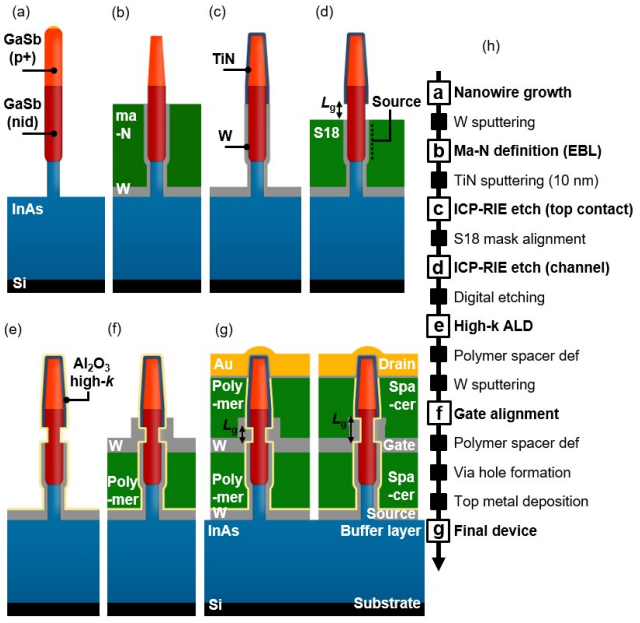

Fig. 1. Schematics for key processing steps realizing gate-length scaling for vertical GaSb p-type MOSFETs. (a) VLS grown hetero-structure GaSb nanowire integrated on an InAs buffer layer on Si. (b) Sputtered tungsten encapsulation aligned by ma-N mask with thickness controlled by EBL. (c) TiN sputtered and removed from planar surfaces by anisotropic etching. (d) S18 spacer aligned by plasma etching and channel region exposed by selective dry etching of W. (e) Cycled oxygen exposure and HCL-IPA dips for recess (digital) etching. (f) S18 polymer spacer aligned by plasma followed by sputtered W with vertical length defined by S18 back-etched mask. (g) Finalized devices after aligning polymer spacer followed by sputtering of drain metal. (e) Itemized overview of the full process-flow.

In this paper, we introduce for the first time a gate-last process [15], [16] for vertical GaSb nanowire MOSFETs that enable gate-length variation. The process is compatible with highly sensitive Sb-based materials [6] that enables a systematical study of scaled p-type MOSFETs in a GAA configuration. The process uses a novel method where the nanowires are fully encapsulated in metal that is selective removed from the sidewalls revealing the channel region. Thus, the sensitive GaSb will remain protected during fabrication and only be exposed prior to the final gate-deposition step. The gate

length is varied from 140 nm to 40 nm at a constant 24 nm channel diameter.

Generally, GaSb transistors exhibit weak modulation properties, with maximum current modulation, at V_{GS} = -0.5V, of barely two order of magnitude considering off-state current. [1], [6], [17], [18] Here, we provide substantially improved current modulation compared to state-of-the-art GaSb based MOSFETs with a maximum on/off-state current ratio I_{on}/I_{off} = 700 (V_{GS} = -0.5 V) . Complete benchmarking of GaSb p-type MOSFETs on Si is summarized in Table I.

TABLE I
BENCHMARKING

	This work	[6] finFET	[1] Sb-sheet	[17] Sb-OI	[18] Sb-OI
L_g [nm]	60	20	500	*	*
Crit.dim.[nm]	24	10	20	7	20
I_{on}/I_{off}	700	50	3000	100	10
$g_{m,max}$ [µS/µm]	50	160	-	-	-
SS_{lin} [mV/dec]	224	260	217	156	-
I_{on} [µA/µm]	20	100	12	-	10
$\|V_{DS}\|$ [V]	0.5	0.5	0.5	1.0	1.0
$\|V_{GS}\|$ [V]	1.0	0.5	1.5	1.0	4.0

Benchmarking comparable and symmetric GaSb [1], [17], [18] and InGaSb [6] p-type MOSFETs on Si. I_{on}/I_{off} defined as the maximum current modulation for stated bias-conditions. MOSFETs within this work showcases good overall performance with the best I_{on}/I_{off} for sub-100 nm L_g devices.

*Long-channel devices (>500 nm), therefore gate-length not disclosed.

II. Device Fabrication

Fig. 1 illustrates the critical fabrication steps for the vertical p-type GaSb MOSFETs. The devices are fabricated on 1 cm^2 p-type silicon (111) substrates with a 260-nm-thick epitaxially grown n^{++}-InAs layer [9], [19]. InAs-GaSb nanowires are subsequently grown from 15-nm-thick Au seed particles, with a diameter of 24 nm, defined by Electron Beam Lithography (EBL). The GaSb top segment (~250 nm) is p-doped by Zn (DEZn/TMGa = 0.36), see Fig. 1a. For GaSb growth, significant background doping (~10^{16} cm^{-3}) is present attributed to point defects [20]. Nanowires for each device are ordered in double-row arrays with 300 nm separation, large enough to avoid capillary coalescence during wet processing [21].

In the first process step, following epitaxial growth, the nanowires are etched in an HCL-IPA oxide etch and then encapsulated in 30 nm sputtered tungsten (W) protecting the GaSb surface from subsequent processing steps. An Ma-N polymer layer (spin-on negative resist, ~500 nm at 2500 rpm) is successively applied to protect the bottom part of the nanowires [9]. Developing the Ma-N with a TMAH based developer gradually etches both the metal and semiconductor leaving an exposed GaSb tapered, top-segment structure, see Fig 1b. The thicknesses of the Ma-N is systematically varied from 200 to 350 nm, by varying the dose in EBL, to define the position of the upper edge of the channel region and thus allow for devices with different gate-lengths. In our previous work, hydrogen silsesquioxane (HSQ) has instead been used to enable gate-length scaling for vertical InAs nanowire MOSFETs [13]. Substituting HSQ (fluidic oxide) with Ma-N (organic spacer) leads to a trade-off, sacrificing thermal and mechanical stability

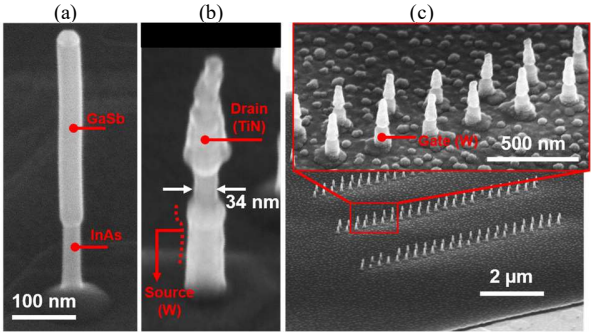

Fig. 2. (a) SEM image of a nanowire implemented in the p-type MOSFET. (b) Device after top and bottom electrode definition. (c) Showcasing a nanowire array contacted by a defined gate-electrode

in order to gain etch selectivity with respect to Sb-based materials. Subsequent to Ma-N definition, 10 nm of TiN is sputtered and anisotropically dry-etched from planar surfaces by SF_6:N_2 finalizing the top contact (Fig 1c). TiN based metals allow for greater anisotropy due to the formation of Ti-F based inhibitors on the nanowire sidewalls [22]. The ma-N mask is stripped by acetone and replaced by an S1813 polymer mask. The polymer mask is thinned in an oxygen plasma to the extent that a segment of the nanowire sidewall, covered with W, protrudes underneath the TiN top contact. An SF6:N2 plasma (ICP-RIE) is used to selectively etch the exposed W, covering the channel region, in between the upper TiN/W layer and the lower S1813 mask, see Fig 1d. The plasma is generated without any forward RF-bias to enable isotropic etching. W forms volatile etch-products in conjunction with SF6 plasma allowing increased etch selectivity between W and TiN when simulating a remote plasma. [22] This etch process step also defines the bottom contact length (Fig 1d), where the InAs-GaSb heterojunction is circumvented by a W socket contact. By only introducing Zn doping (in-situ) at the top of the GaSb segment, excess dopants within the channel region can be avoided [23]. Therefore, the bottom contact relies on the comparably high backgroung doping (~10^{16} cm^{-3}) present in the GaSb [20].

The S1813 mask is stripped by acetone leaving the finished top and bottom metal contacts. This allows for selective digital etching of the channel by oxidation inside an O_2-chamber followed by an HCL:IPA (1:10) oxide etch. The digital etch cycles are repeated until the nanowire diameter is reduced from 36 nm down to 24 nm, as confirmed by SEM inspections. Using

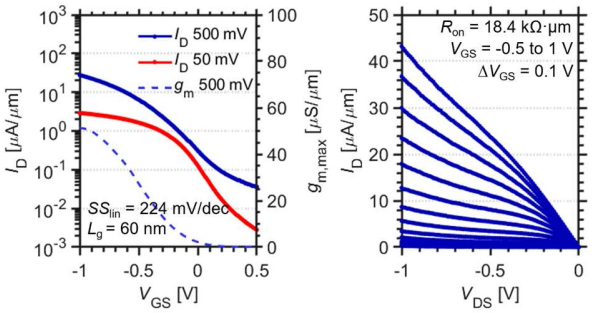

Fig. 3. Transfer and output characteristics for a MOSFET with 60 nm gate-length demonstrating a maximum transconductance of 50 uS/um at V_{DS} = -0.5 V.

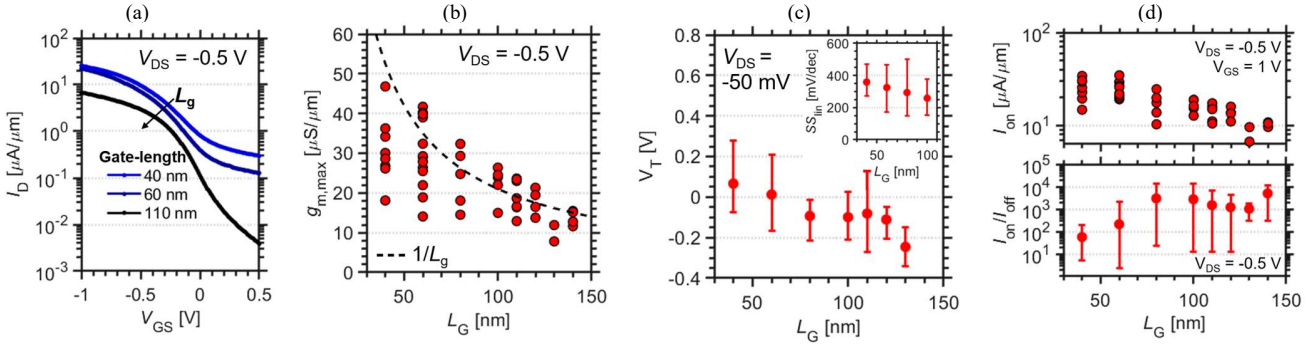

Fig. 4. Statistic for the vertical p-type GaSb MOSFETs based on 42 separate devices. (a) Full transfer characteristics for representative devices at varied L_g. (b) Maximum transconductance versus L_g at V_{DS} = -0.5 V, dashed line representing expected trend with respect to drift diffusion ($1/L_g$). (c) Threshold voltage behaviour at varying Lg with an inset representing linear subthreshold swing SS_{lin}. (d) I_{on} for 42 individual devices with respect to L_g and modulation I_{on}/I_{off} at V_{DS} = -0.5 V as a function of L_g with I_{on} defined at V_{GS} = -1 V and I_{off} at V_{GS} = 0.5 V.

O_2 environment for oxidizing of the GaSb stabilizes the digital etch rate [6], thus we believe that diameter variation between nanowires originate mainly from variation during epitaxial growth (±2nm) [24]. A 50 cycle ALD film of Al_2O_3, deposited at 300° C, high-k (50 Å, EOT = 1.9 nm) [25] is applied (Fig 1e) followed by a 100-nm-thick back-etched S1813 resist acting as a bottom spacer. The gate metal is formed by sputtering of 60 nm W followed by a thinned S1813 mask for an SF6 dry-etch process to vertically define the gate overlap re-revealing the top contact, see Fig 1f. A final polymer spacer is defined followed by a top metal electrode consisting of Ni/Au finishing and capping the device, see schematic in Fig. 1g.

The results at separate process steps are verified by SEM-inspections shown in Fig 2. Post-growth inspections show a 500-nm-long heterostructure InAs-GaSb nanowire (Fig 2a). After the critical stage of contact formation, recess etching, and high-k (5 nm Al_2O_3) deposition a 34 nm neck region is exposed that is corresponding to a 24 nm diameter channel-region (Fig 2b). Even after aligning the gate and re-revealing the top contact, an excellent yield for the full nanowire array is realized (Fig 2c).

III. Device Characterization

Transfer and output characteristics for a vertical GaSb nanowire MOSFET, with L_g = 60 nm, is presented in Fig 3. A peak transconductance $g_{m,peak}$ value of 50 μS/μm with minimum subthreshold slope SS_{lin} of 224 mV/dec is achieved. A large current modulation, over several decades, with maximum I_{on}/I_{off} = 700 (V_{GS} = -0.5V) is also realized. The device demonstrates well behaved output characteristics, although a large on-resistance R_{on} of 18.4 kΩ·μm is present.

Fig 4. presents transfer characteristics and also statistics for key performance metrics with respect to gate-length scaling for 49 devices. Transfer characteristics for transistors with varying gate-lengths is presented in Fig 4a. For shorter L_g the on-state improves while the off-state performance is sacrificed due to degraded electrostatics, considering a fairly large diameter of 24 nm and EOT at 1.9 nm (calculated based on cylindrical oxide capacitance). I_{off} (at V_{DS} = 0.2 V) and saturation subthreshold swing SS_{sat} (at V_{DS} = -0.5 V) vary from 3.8 to 297 nA/μm and 216 to 393 mV/dec, respectively. Statistics with respect to maximum transconductance $g_{m,max}$ vs L_g is presented in Fig 4b. A clear correlation between L_g and $g_{m,max}$ is evident where shorter gate-lengths lead to improved on-state performance. Performance variation can be mainly attributed to varied contact resistance, originating from the reactive nature of GaSb surfaces [26]. Therefore, varied access-resistance is naturally more detrimental to the short gate-length devices (L_g < 100 nm) which exhibit greater on-state performance. Fig. 4c. demonstrates V_T and SS_{lin} (point slope) behavior with respect to L_g. A clear V_T roll-off is seen at shorter gate-length as well as degraded electrostatics described by SS_{lin} attributed to the unfavorable channel/gate aspect ratio (2:1) at shorter L_g as well as relatively large EOT leading to short-channel effects (SCE). [27] According to scaling theory for cylindrical GAA MOSFET, a five-times larger gate length is required with respect to field penetration λ_n (calculated to 15 nm) to retain electrostatic control [28], [29], in this case corresponding to a channel/gate aspect ratio of 3:1. Despite SCE, the VT roll-off of 200 mV, for L_g = 40 to 100 nm, is significantly reduced due to the GAA geometry as compared to finFET structures demonstrating a 600 mV shift for fin-widths of 26 nm [6]. Fig. 4d. presents on-current I_{on} and modulation properties I_{on}/I_{off} with respect to L_g for the devices. Smaller L_g grants increased I_{on} attributed to a decrease in channel-resistance. The L_g-scaling is more prevalent for the transistors modulation, demonstrating I_{on}/I_{off} up to 4 orders of magnitude (I_{on} and I_{off} at -1 and 0.2 V respectively).

The systematic gate-length variation also enables determination of contact resistance from R_{on} vs L_g for 18 similar devices, see Fig. 5a. A linear increase in on-resistance is observed when increasing the gate-length, which enables an extrapolation to 20 kΩ·μm of the total contact resistance R_{sd}. Inset shows the g_m vs L_g for the specific p-type devices, increasing for shorter L_g. Transconductance is in fact comparable (within 10%) when reversing the source and drain electrodes indicating symmetrical device with respect to contact resistance, namely providing similar source and drain resistance. By studying the behaviour of the output characteristics with respect to L_g, see Fig. 5b, a model can be applied in the linear region (see inset). The model is based on drift diffusion considering contact resistances as $I_D = kV_{ov}V_{DS}/(L_g+kV_{ov}R_{sd})$ with overdrive voltage $V_{ov}=V_{GS}-V_T$ and physical parameters contained in $k = W_{eff}\mu_h C_{inv}$ with effective

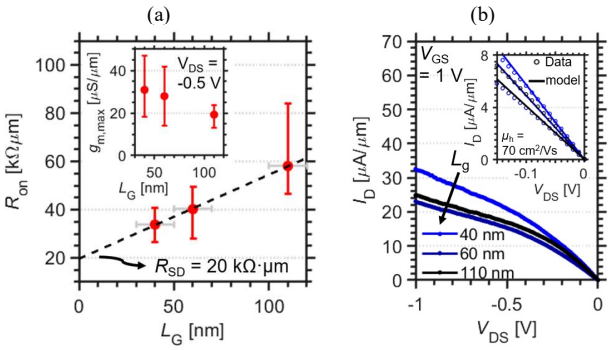

Fig. 5. Statistics and output characteristics for 18 similar devices (same chip location). (a) Extrapolation of contact resistance from R_{on} vs L_g. (a) Output characteristics for L_g at 40, 60 and 110 nm. Inset shows fitted model for the linear region considering source and drain resistance resulting in a hole-mobility of 70 cm²/Vs.

gate width W_{eff}, hole mobility μ_h, and inversion capacitance C_{inv}. With R_{sd} = 20 kΩ·μm and C_{inv} = 0.5 aF/nm (calculated considering a coaxial capacitance) the effective hole mobility is determined to μ_h= 70 cm²/Vs. [30] Earlier work based on vapor-liquid-solid (VLS) grown GaSb nanowires reported a field-effect mobility varying between 50-100 cm²/Vs [20] well in line with our reported values considering that surface effects dominate transport in thin nanowires (< 24 nm diameter) [31], [32].

The EOT, at 1.97 nm, of the devices can be considered large in comparison to previous vertical NW MOSFET technology where an EOT below 1 nm have been demonstrated [33]. This implies that a 2*x* increase in performance can be expected by simply high-*k* optimization. Further, the large contact resistances (R_{sd} = 20 kΩ·μm) can be addressed by passivation techniques [32], [34] and heterostructure growth using core-shell structures [6], [35]. The intrinsic channel properties can also be improved by growth and strain engineering [36], [37]. Nonetheless, our novel fabrication techniques paves the way for the next generation of p-type MOSFETs and grants extended design freedom with respect to Sb-based materials.

IV. Conclusions

A new process scheme for vertical p-type (GaSb) MOSFETs has been developed to enable systematic gate-length variation, from 40 up to 140 nm. Fabricated devices demonstrate excellent modulation properties and improved electrostatic control, which is further enforced by a comparably small V_T roll-off. Improved yield enables a significant data set for analysis of both contact and transport properties. Strong modulation properties I_{on}/I_{off} up to 4 orders of magnitude are also realized. To further elevate performance of the GaSb p-type MOSFET various passivation techniques and core-shell contacts can be implemented.

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